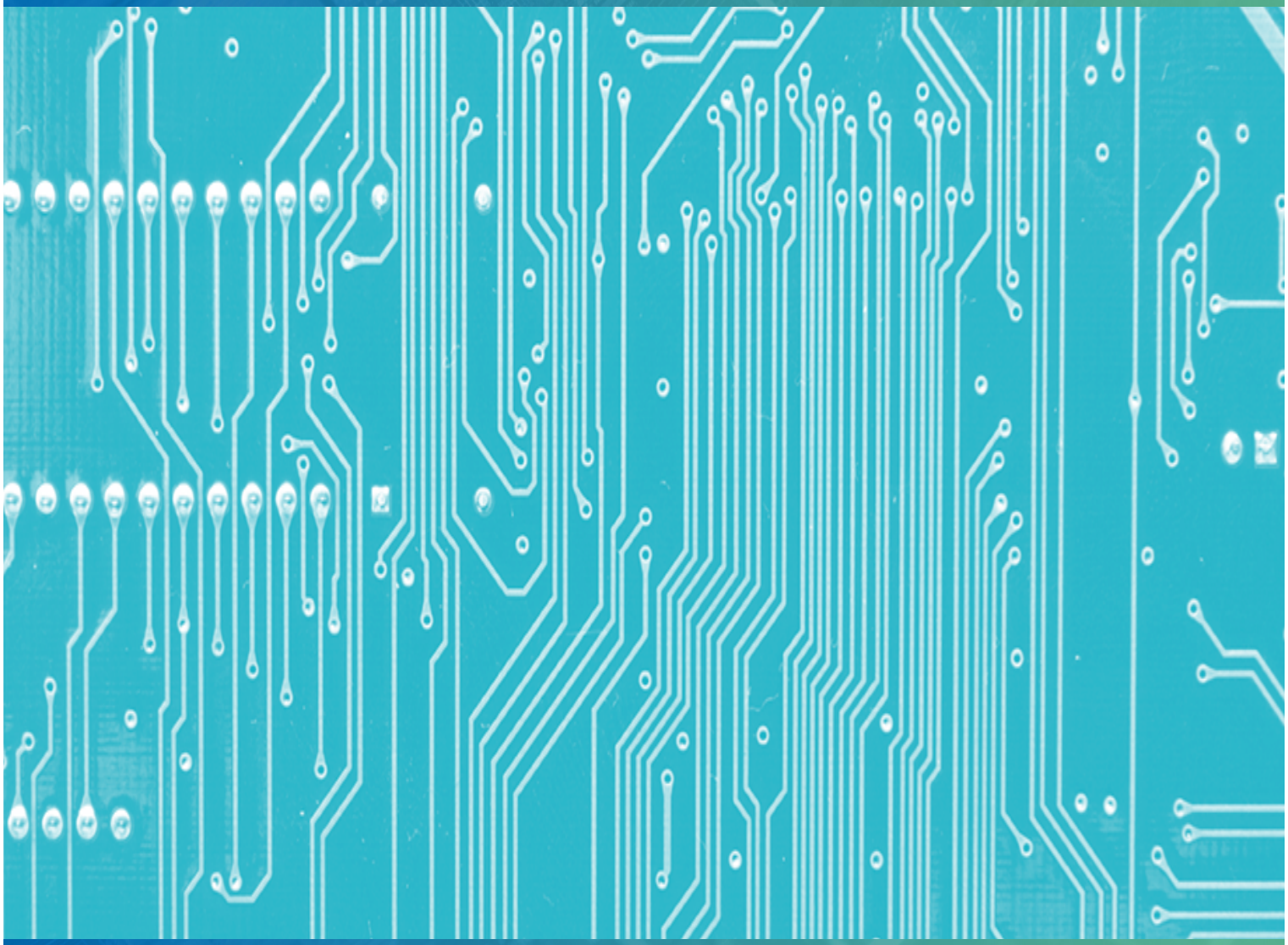
Una Aproximación Multinivel al Diseño Sistemático de Circuitos Integrados de Radiofrecuencia



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1

Introduction

In an emerging telecommunications market, evolving towards 5G [1], it is estimated that there are over 2 billion smartphones users nowadays [2]. Only by itself, this number is astonishing. But nothing compares to what is going to happen in the near future. The next technological boom is directly related to the emerging internet-of-things (IoT) market. It is estimated that by 2020, there will be 20 billion physical devices connected and communicating with each other [3], which gives more than 2 physical devices per person on the planet. Due to this technological boom, new and interesting investment and research opportunities will emerge. In fact, it is estimated that in 2020 approximately 3 billion dollars will be invested in this market alone, 50% more than in 2017 [3]. Due to the fact that most of these IoT devices will have to communicate wirelessly among each other, and that radio-frequency (RF) circuits are essential for that purpose, there is, and there will be a high demand for RF circuits, nowadays and in the foreseeing years. Therefore, it is easy to understand why integrated chip (IC) design companies specialized in RF, are already the companies which generate more income among all the fabless IC suppliers (e.g., Qualcomm and Broadcom, see Fig. 1.1).

The problem is that the design of RF circuits in nanometric technologies is becoming extremely difficult due to its increasing complexity. Designing an RF circuit is one of the most challenging tasks in nowadays electronics, due, partially, to its demanding specifications, convoluted trade-offs and high operating frequencies. In fact, compared to its analog (baseband) and digital counterparts, the RF design requires a higher design effort despite the comparatively low number of devices (see Fig. 1.2). With todays' strict time-to-market restrictions and the need for design solutions with very demanding performance specifications, one of the areas where it is extremely important to focus is on the development of new systematic design methodologies for RF circuits. These RF circuit design methodologies must allow the designer to obtain circuits which comply with the demanding

2017E Top 10 Fabless/System IC Companies ($M)

2017E Rank	Company	Headquarters	2016 Tot IC	2017E Tot IC	2017/2016 % Change
1	Qualcomm	U.S.	15,414	17,078	11%
2	Broadcom Ltd.	Singapore	13,846	16,065	16%
3	Nvidia	U.S.	6,389	9,228	44%
4	MediaTek	Taiwan	8,809	7,875	-11%
5	Apple*	U.S.	6,493	6,660	3%
6	AMD	U.S.	4,272	5,249	23%
7	HiSilicon	China	3,910	4,715	21%
8	Xilinx	U.S.	2,311	2,475	7%
9	Marvell	U.S.	2,407	2,390	-1%
10	Unigroup**	China	1,880	2,050	9%
—	Top 10 Total	—	65,731	73,785	12%
—	Other	—	24,694	26,825	9%
—	Total Fabless/System	—	90,425	100,610	11%

*Custom ICs provided by foundries for internal use.
**Includes Spreadtrum and RDA
Source: Company reports, IC Insights' *Strategic Reviews* database

Figure 1.1: Illustration of the top 10 ranking of fabless IC suppliers for 2017 [4].

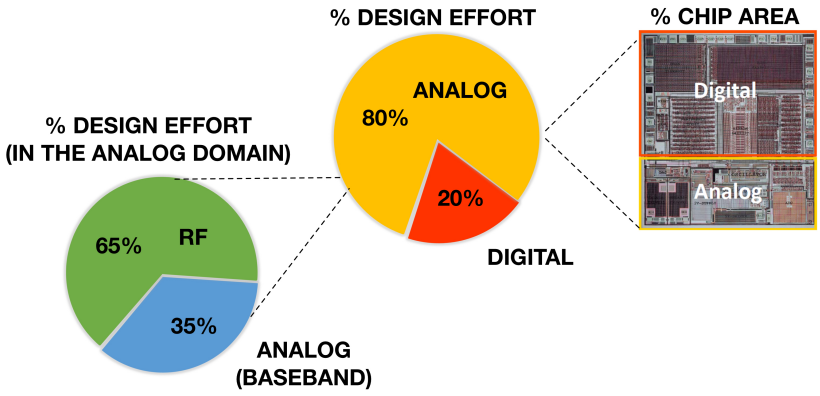


Figure 1.2: Illustration of the design effort comparison between analog and digital, and between analog (baseband) and RF. Illustration of the area differences between the analog and digital parts.

specifications in a reasonable time.

1.1. Traditional Design Methodologies

In the analog and RF domain, the traditional design methodology follows the flow illustrated in Fig. 1.3. The design of an IC starts by the definition of the circuit performances that have to be achieved, and then, the so-called electrical and physical synthesis have to be performed. These synthesis stages compose the core of any design flow and are the most important stages of any circuit design methodology. The first step of the flow is the electrical synthesis, where the designer must select an appropriate circuit topology and *size* the design. This *sizing* operation is a process where the designer finds the dimensions of each device used (transistors, capacitors, etc.) in order to meet the desired specifications. The output of this electrical synthesis is a schematic, which contains a list of all

the devices composing the circuit and how they are connected. Furthermore, and more importantly, this schematic also includes the sizes of each single device (e.g., transistor lengths and widths, etc.). After the electrical synthesis is performed, the physical synthesis must be achieved. The goal of this step is to attain the physical representation of the circuit, known as layout. This layout is a collection of geometric shapes and layers which are later used for fabrication. After the physical synthesis, the layout of the circuit must be verified, and, if valid, it is ready for fabrication. If not, some re-design stages are needed.

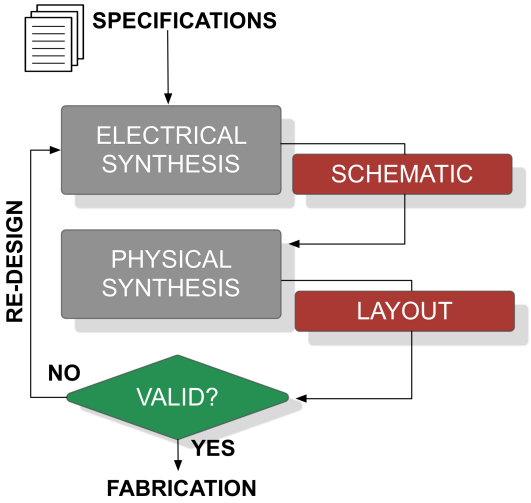


Figure 1.3: Electrical and physical synthesis.

If the circuit/system under design is too complex, analog/RF designers use divide-and-conquer techniques in order to reduce the complexity of the entire system. The basic idea is to partition the system into smaller pieces, which are easier to manage. This is known as hierarchical partitioning. The most well-known hierarchical design strategies are the top-down and bottom-up design methodologies, as shown in Fig. 1.4.

In top-down design methodologies, the designer starts by designing the system level, and the performances are consecutively derived for the lower levels, until reaching the device level. The circuit is designed in a more ”abstract” way in high-levels, relying in e.g., behavioral simulations, and, at lower-levels, more precise simulations can be performed. Furthermore, at each level of the design hierarchy, a verification stage must be performed in order to check if the design is valid. One of the advantages of top-down methodologies is that the specifications for the entire system are known since an initial design stage (although only estimated). However, if any of the circuits composing the system do not attain the necessary performances, some re-design iterations are needed in order to achieve the desired specifications. In the worst possible scenario, the complete system architecture must be changed. On the other hand, in bottom-up design methodologies, the design stage starts by the device-level and ends up in the system-level. The main disadvantage of bottom-up methodologies is that the system performances are only verified when all its composing blocks are designed, which can

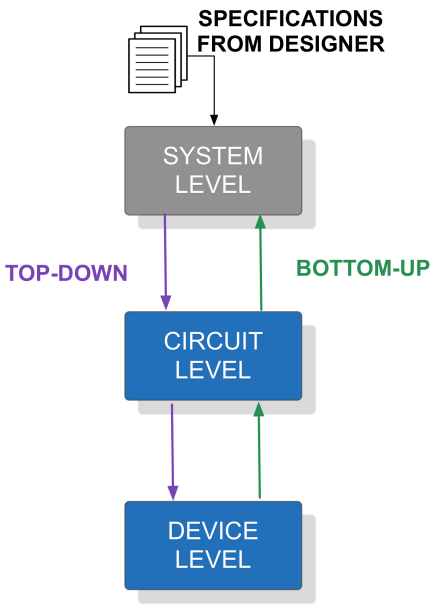


Figure 1.4: Top-down vs. bottom-up design methodologies.

lead to major design changes later in the design process.

In practice, the basic idea of traditional design methodologies, is that, at each level of the hierarchy, the designer must perform a top-down electrical synthesis and a bottom-up physical synthesis, both needing a verification stage, as shown in Fig. 1.5.

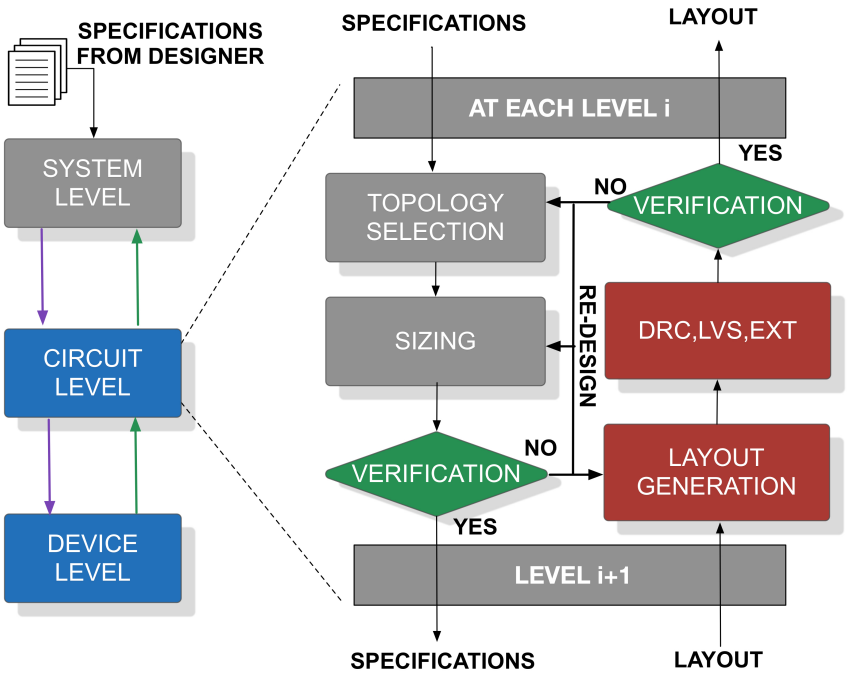


Figure 1.5: General design flow for analog and RF integrated circuits.

As part of the electrical synthesis, the designer must select the architecture/topology which is capable of achieving the desired specifications. Afterwards, the sizing process in performed. At higher

levels, the sizing is the process of mapping the current level specifications into the needed specifications for the immediately lower level. At device level, sizing is the process of dimensioning each passive and active circuit component. After the topology selection and sizing operation, the design is simulated and verified in order to check if the specifications are met. If the specifications are met, the flow continues to the next level.

The physical synthesis involves the layout generation stage, where the layout of a device, or circuit is generated. Afterwards, the layout is checked against a set of technology-defined rules with a design-rule check (DRC), and a layout-versus-schematic (LVS) check is performed, and if both checks are valid, the layout is acceptable for fabrication. However, a parasitic extraction (EXT) must be performed. This is important in order to extract the layout-induced effects. These layout-induced effects add a set of capacitances, resistances and inductances to the circuit, and therefore, may change its performances. If the specification are not met after the layout extraction, the layout must be performed again or, in a worse scenario, a re-sizing operation must be performed. The illustration of the complete hierarchical design for the levels of abstraction previously discussed (system, circuit and device), is shown in Fig. 1.5.

All steps of the hierarchical flow shown in Fig. 1.5, can undertake several re-design iterations in order to reach the final system design that meets all specifications, therefore making the process of designing an IC a long and (usually) repetitive task. Hence, in order to relieve the designer from these long and repetitive tasks, the IC design process can be automated. In an ideal scenario, designers would have an electronic design automation (EDA) tool that could automatically perform the steps demonstrated in Fig. 1.5, something defined as a silicon compiler [5]. With this ideal tool, the user would only stipulate the desired specifications for his/her system and the tool would automatically generate the IC ready for fabrication. However, such a tool does not exist. In the digital domain the automatic circuit design tools are relatively close to the previously described silicon compiler. However, in the analog domain, and especially in RF, this silicon compiler is yet nothing but a dream.

Therefore, the main topic of this dissertation is to focus on the development of new systematic design methodologies capable of improving the state-of-the-art and cut short the distance between the RF and digital automatic design tools. By doing so, it will be possible to shorten the existing productivity design gap in RF circuit design.

In Section 1.2 a brief historical background on automatic circuit design is performed, and the current state-of-the-art is overviewed. In order to establish a new design methodology for RF systems, different bottlenecks of the RF design process must be addressed in order to successfully design such circuits. Hence, in Section 1.3, the demands for an accurate RF system design methodology are discussed. The issues tackled by this thesis and the proposed innovative contributions are illustrated in Section 1.4 and, in Section 1.5, the publications and achievements accomplished during the author's doctoral studies are presented.

1.2. Automatic Circuit Design State-of-the-art

In this Section the state-of-the-art on automatic circuit design methodologies is reviewed. As previously mentioned, the electrical and physical synthesis are the core of any design methodology and therefore, the state-of-the-art for both of them is reviewed.

1.2.1. Knowledge-Based Approaches

The basic idea of knowledge-based approaches is to have a pre-defined design plan, in the form of design equations or design strategies, to find the circuit sizing/layout so that the specifications are met. These type of tools are known as knowledge-based approaches because they use knowledge and expertise from the designer in order to establish/define a design plan for a given circuit.

Knowledge-Based Electrical Synthesis

In the 90's, several tools were developed which could automatically perform electrical synthesis of analog circuits [6–10]. In these tools, the design plan was basically a set of analytical equations, which were used to solve the circuit. The tool provided the means to automatically execute a routine that would solve all the equations and therefore size the circuit under study. The main advantage of these approaches is its short execution time. However, deriving the design plan is hard and time-consuming, the derived equations are usually too simple and do not incorporate all the device physics. Moreover, the design plan requires constant maintenance in order to keep it up to date with technological evolution, and the results are not optimal, suitable only as a first-cut design.

Knowledge-Based Physical Synthesis

In order to perform circuit physical synthesis, other knowledge-based tools, were also developed. Roughly, the phases of layout generation are $placement$, where all circuit components are distributed over the layout plane (also called floorplan), and $routing$, where all components are interconnected. Automatic knowledge-based layout generation tools, were developed in order to generate the circuit layout in such a way that placement and routing were specified in advance. There are two types of knowledge-based approaches for automatic layout generation: rule-based and template-based approaches. Rule-based approaches use a set of rules, that have to be followed by whichever placement and routing algorithms are used during circuit layout generation [11]. In template-based approaches, the main idea is to capture the designer expertise in a template that specifies all necessary component floorplanning and the routing spatial relationships. Moreover, the template, must capture analog specific constraints like routing symmetry and device matching [12].

1.2.2. Optimization-Based Approaches

Knowledge-based design tools were developed in order to automatize some of the tasks inherent to analog/RF designers, without aiming at optimality. In order to reach optimal designs, optimization algorithms can be used in order to perform electrical/physical synthesis. The design of any

circuit/system can be posed as an optimization problem, mathematically defined as

$$\begin{aligned} \text{minimize} \quad & \mathrm{f(x)}; \quad \mathrm{f(x)}=\{f_1(x), f_2(x), ..., f_n(x)\} \in \mathbb{R}^n \\ \text{such that} \quad & \mathrm{g(x)} \geq 0; \quad \mathrm{g(x)}=\{g_1(x), g_2(x), ..., g_m(x)\} \in \mathbb{R}^m \\ \text{where} \quad & \mathrm{x}_{Li} \geq x_i \geq x_{Ui}, \; i \in [1, p] \end{aligned} \tag{1.1}$$

where x is a vector with p design parameters, each design parameter being restricted between a lower limit x_{Li} and an upper limit x_{Ui}. The functions f_j, with $1 \leq j \leq n$, are the objectives that will be optimized, where n is the total number of objectives. The functions g_k, with $1 \leq k \leq m$, are design constraints. The basic approach to solve Eq. (1.1) is illustrated in Fig. 1.6. It is possible to observe that the optimization algorithm is linked with a performance estimator, where the designer chooses the circuit performances to be considered (optimization objectives and constraints) and executes the algorithm which then returns the circuit sizing (e.g., widths and lengths of transistors).

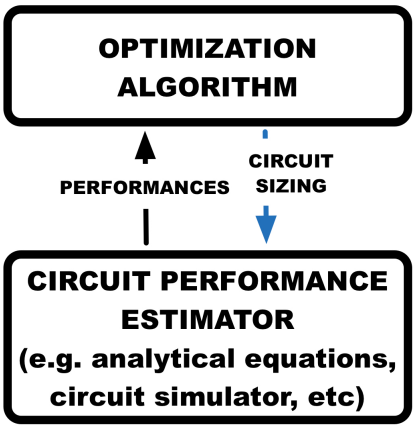


Figure 1.6: Optimization-based methodology for circuit design

Optimization-Based Electrical Synthesis

While performing optimization-based electrical synthesis, there are two main categories, namely, equation-based and simulation-based.

The equation-based methods use analytical equations in order to evaluate the circuit performances. Several tools were developed which implemented this method [13–21]. Equation-based optimization-based sizing is similar to the knowledge-based sizing methods in the sense that they both use relatively simple analytical equations in order to estimate the circuit performances. However, equation-based methodologies do not need an explicit ”design plan” to be defined. Also, the methods presented in this Section go a step further by linking the equations with optimization algorithms, which were developed in order to reach optimal results. Similarly to the knowledge-based approaches, the advantage of equation-based methods is the short evaluation time. These methods are extremely suitable to find first-cut designs. However, like the knowledge-based approaches, the main drawback is that not all physical characteristics of the devices can be easily captured by analytic equations, making the method

inaccurate (especially for RF circuits) and the generalization to different circuits, technologies and specifications is very time-consuming because new equations have to be derived.

Equation-based optimization methodologies are suitable because they are computationally cheap and therefore very fast to evaluate, and can be used in order to achieve first-cut designs. However, they lack sufficient accuracy. Therefore, instead of using analytical equations in order to estimate the circuit performances, a circuit simulator (e.g., electrical simulator [22]) should be used in order to accurately estimate the circuit performances. The advantage is that these type of simulators tend to be much more accurate than analytical equations. The methods linking an optimization algorithm with a circuit simulator are usually defined as simulation-based strategies. Therefore, in order to obtain more accurate designs, these simulation-based optimization gained ground and became the most common optimization-based strategy. Some of the developed works that employ these simulation-based sizing methods can be found in [23–40].

Optimization-Based Physical Synthesis

Several tools have been developed that are able to perform physical synthesis using optimization-based approaches. With such tools, placement and routing stages of the layout generation are determined by an optimization algorithm according to a certain cost function. This cost function typically considers the minimization of some design aspect, such as, layout area or routing length. Furthermore, some constraints may be used in order to penalize the violation of some analog/RF design constraints, such as symmetrical RF signal paths, device mismatch, etc.

Some of the developed tools, the so-called heuristic approaches, are able to automatically generate layouts from circuit descriptions, while handling typical layout constraints such as, device matching, symmetry, etc. However, these approaches do not account for the performance degradation that appear due to devices physical implementation [41]. Therefore, they do not provide promising results because the layout parasitic effects, which highly degrade the performances of the circuits, are not taken into account during the design stage. Therefore, one of the keys in order to have a successful circuit synthesis is that the electrical synthesis and the physical synthesis should not be considered as separate steps of the design methodology. Hence, new optimization-based physical synthesis approaches appeared, the so-called performance-driven. In these approaches, the layout-induced effects are taken into account [42]. These performance-driven tools try to measure the layout-induced degradation and keep it below desired margins. Thus, the impact of each layout parasitic is weighed out according to its effect on the circuit performance.

1.2.3. Hierarchical Optimization-Based Approaches

Similarly to what happens in the traditional circuit design flow, the divide-and-conquer techniques can also be used in optimization-based methodologies in order to ease the optimization and therefore the design process. This kind of divide-and-conquer techniques are particular useful, because, when the problem is too complex (e.g., too many design variables), optimization algorithms struggle to converge

to optimal solutions, and the process can become inefficient. Therefore, the previously described top-down and bottom-up design strategies can be applied to optimization-based design methodologies

The top-down design methodologies are illustrated in Fig. 1.7. In top-down design methodologies the designer sets the specification for the highest level (e.g., system level). During the high-level optimization, the "design variables" are the performances for the lower-level circuits. After obtaining the high-level design, the performances for the lower-levels (e.g., Sub-block 1, Sub-block 2, etc.), must be attained, and this process continues down to the lowest-level of the hierarchy (e.g., SB1.1, SB1.2, etc.). Several works used these type of design methodology [31, 33].

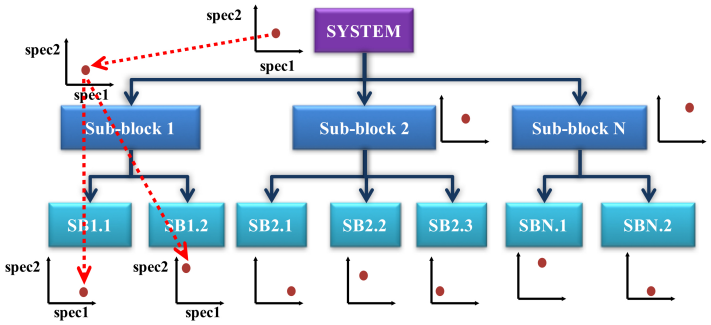


Figure 1.7: Top-down design methodologies

The problem with this kind of methodologies is that the designer usually uses a system level design tool in order to obtain the specifications of lower level blocks. Afterwards, when the designer tries to synthesize the lower-level blocks, it may happen that some of the needed specifications are impossible to meet and therefore, re-design cycles are needed, which will degrade the efficiency of the entire process.

In order to reduce, or even eliminate, the re-design cycles, bottom-up design methodologies can be used. Fig. 1.8 illustrate this type of methodologies. The main idea in bottom-up methodologies is to start designing the system from the circuit-level (e.g., SB1.1, SB1.2, etc.) until reaching the system-level. Several different works employed this methodology [35–40].

Both top-down and bottom-up design methodologies can be assisted by several different optimization algorithms. In top-down methodologies, the design variables at each level are usually the performances for lower levels. Therefore, when the designer optimizes the lower level, he/she is trying to synthesize those performances. In order to do so, single-objective optimization algorithms are commonly used (n=1 in Eq. (1.1)). Therefore, at each level the designer would achieve only one design (illustrated by the dot at each level of Fig. 1.7). However, in bottom-up design methodologies the use of single-objective optimization algorithms is impossible because, when going from lower to higher levels the designer does not know *a priori* which performances he/she is looking for in order to satisfy the system specifications. Therefore, multi-objective optimization algorithms must be used (n>1 in Eq. (1.1)). While the solution to the single-objective optimization algorithms is a single

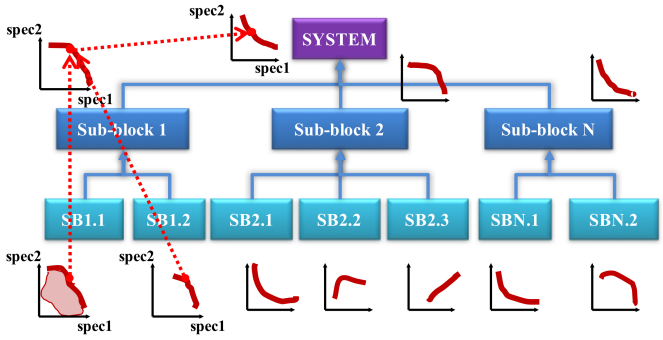


Figure 1.8: Bottom-up design methodologies

design point, the solution to the multi-objective optimization algorithms is a set of solutions exhibiting the best trade-offs between the objectives (illustrated by the curve at each level of Fig. 1.8, for a case with two objectives). Therefore, when synthesizing a given high-level block, the design space of that optimization is set by the designs available from lower levels. In practical terms, what the designer is doing with these methodologies, is exploring the design space of each level and finding the optimal designs for that level, hence, building an optimized library for each device/circuit/system.

When discussing multi-objective optimization algorithms, a few key concepts must be first established. In single-objective optimization algorithms, the final obtained solution can be considered the best one because it is the one that achieved the ”best” value for the objective function value $f(x)$. However, for multi-objective optimization this cannot be performed because there are several objectives. Therefore a new concept must be established. This concept is denoted as Pareto dominance. A design point a is considered to *dominate* the design point b, if $f(a) \leq f(b)$ and $f_i(a) < f_i(b)$ for at least one objective i (for minimization problems). The design point a is said to be non-dominated if there is no other design point that dominates it. The non-dominated set of the entire feasible[1] search space is known as Pareto set, exhibiting the best trade-offs between the objectives, i.e., the Pareto optimal front (POF). The concept of Pareto dominance and the Pareto optimal front are described in Fig. 1.9 for a problem where both $f_1(x)$ and $f_2(x)$ are minimized. It is possible to see that y^a is non-dominated and Pareto optimal because $f_2^a(x)$ and $f_1^a(x)$ are lower than $f_2^{b,c}(x)$ and $f_1^{b,c}(x)$.

These multi-objective optimization algorithms are extremely useful since the circuit sizing is in its essence a multi-objective problem, and the designer often wants to explore the trade-offs among conflicting performances, for example, the power consumption versus gain of a low noise amplifier.

[1]A feasible point is a point that complies with the constraints of the optimization problem

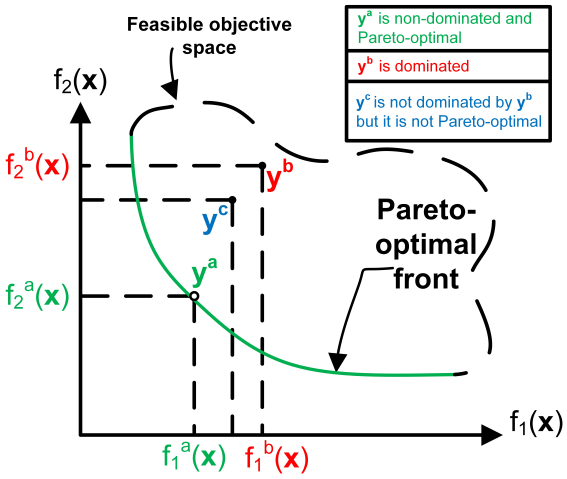


Figure 1.9: Illustrating Pareto dominance and Pareto-optimal front concepts for a 2-dimensional performance space

1.3. Demands for an Accurate RF Automatic Circuit Design Methodology

From all the cited works so far, most of them are centered on the analog and mixed-signal domain, and only a few of them found its path to the RF world (e.g., [28, 32, 35, 40]). The design (and consequently automation) of RF circuits if far more complex and delicate than the analog ones due to several reasons. The difference between baseband and RF is largely due to the fact that capacitive and inductive reactances tend to be more significant at high frequencies than they are at lower frequencies. At the lower frequencies, those reactances exist, but they can usually be ignored. On the other hand, at RF frequencies, the parasitic or distributed reactances tend to be significantly high in order to establish resonance. Another fact that highly affects the automation of RF circuit design is the time and accuracy of the analysis needed. The analysis needed to estimate the RF circuit performances are more time-consuming than the ones used in the analog baseband domain (e.g., AC analysis vs. periodic steady-state analysis). Furthermore, techniques such as periodic steady-state (PSS), have only been available in the last few years, leaving early RF designers with limited options such as transient analysis, which is highly time-consuming. Also, in the past, the available techniques used in order to calculate performances like e.g., circuit noise were fuzzy and sometimes inaccurate [32].

Even in modern times, with modern commercial SPICE-like simulators, the efficiency of optimization-based approaches can be hampered due to convergence issues in analysis such as PSS and, performances such as IIP_3 usually need power sweeps, which highly decrease the efficiency of the optimization process. Therefore, it can be concluded that developing an efficient automated circuit design methodology is not an easy task. In order to develop an accurate automated RF circuit design methodology some of the biggest bottlenecks are: the accurate modeling of passive components such as integrated inductors, the layout-parasitics that are very important in RF

frequencies, and the process variability which highly affects nanometer technologies. Another important issue, is the circuit complexity that the methodology is able to cope with. Most of the automated circuit design methodologies presented in literature are only suited for the RF block level design. When the system level is reached, designers usually use high-level simulation tools in order to estimate performances. However, these high-level tools may introduce some deviation from an actual transistor-level simulation. This fact is even more important in RF, because accuracy is a must.

In the next Sections the issues that must be tackled in order to develop an accurate and efficient automated RF IC design methodology are discussed in detail.

1.3.1. Circuit Performance Evaluation

In RF design, evaluating the circuit performances with analytical equations is not a valid approach because they are simply not sufficiently accurate. RF circuits are extremely sensitive to any performance deviation, which may cause the circuit to malfunction. Therefore, RF circuit simulators must be used, such as SpectreRF [43], EldoRF [44] or HspiceRF [45]. Commercial SPICE-like circuit simulators are probably the most established CAD tool in the RF design flow, being used to verify the performance of the circuit since the early design stages until post-layout validations. Therefore, this is a mandatory requirement for high accuracy. However, some analysis are lengthy and can have convergence problems, as mentioned before. Therefore, the designer must use/develop efficient simulation strategies for each performance.

1.3.2. Integrated Inductor Modeling and Synthesis

In nowadays RF ICs, passive components play a key role in circuit design for impedance matching, tuning, filtering, or biasing. For example, it is estimated that in a cellular phone, passive components account for 90% of the component count, 80% of the size, and 70% of the cost [46]. From all passive components (e.g., resistors, capacitors and inductors), while resistors and capacitors are accurately modeled in CMOS technologies, inductors are still a bottleneck for designers. Several authors discussed the inclusion of inductors' performances during their optimization methodologies using several different strategies. The most straightforward option is to use foundry-provided inductor libraries/models, as performed in [28, 40, 47] (see Fig. 1.10 (a)).

However, these models usually do not provide sufficient accuracy for these passive components. Furthermore, if an inductor library is provided by the foundry, it is usually a limitative option because it reduces the possibility of finding an optimal inductor for a given application. Therefore, some authors fancy using simulators/models that are able to relate performance parameters with the inductor geometric parameters, which provide a wider range of inductor choices. The most accurate inductor evaluator (electromagnetic (EM) simulator) was used in [48] (see Fig. 1.10 (b)). However, EM simulations are very time-consuming and, therefore, including them in an optimization-based process, where thousands of simulations must be performed, makes it an inefficient option.

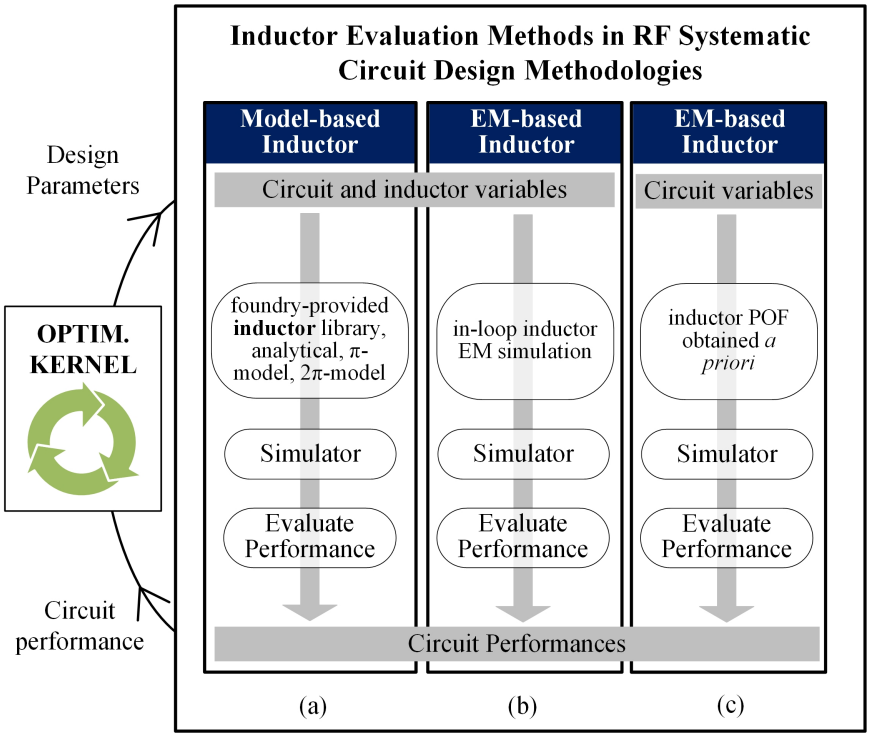


Figure 1.10: Differences between inductor evaluation techniques in systematic circuit design methodologies ((a) Model-based inductor, (b) EM-based inductor) and bottom-up systematic circuit design methodologies ((c) EM-based inductor).

Moreover, the circuit designed in [48], has only one inductor. If a circuit with more inductors is needed, the number of EM simulations would increase, converting this method into an unaffordable one. On the other hand, analytical/physical models are able to calculate inductor performances very efficiently. In [49] a compact model is used to incorporate the inductor performances during the optimization of RF power amplifiers. Similar methodologies use inductor analytical models, such as the π-model (see Fig. 1.11 [50]) [30, 51, 52] or 2π-model [53] (see Fig. 1.10 (a)). However, most of the analytical models do not present sufficient accuracy, especially at high frequencies [54]. As a way of achieving EM accuracy but avoiding EM simulations during the optimization of a given circuit, in [35, 55] a Pareto optimal front (POF) of EM simulated inductors is obtained prior to any circuit optimization, and then, the inductor POF is used as optimal design space during a given circuit optimization (see Fig. 1.10 (c)). By doing so, the inductors are modeled with EM accuracy and no EM simulation is performed during a circuit optimization, reducing therefore the total circuit design time. Furthermore, the POF has to be generated only once for a given inductor topology and operating frequency, and can later be used in several circuit optimizations. However, even though the inductor POF generation is only performed once for a given topology and operating frequency, the generation of the POF could still take weeks. Hence, if a new inductor topology is needed, or the circuit operating frequency changes, a new inductor POF has to be generated, which is a very lengthy process.

In the last few years, surrogate inductor models have risen as an attractive alternative aimed at combining the efficiency of analytical models with the accuracy of EM simulation [54]. Surrogate models

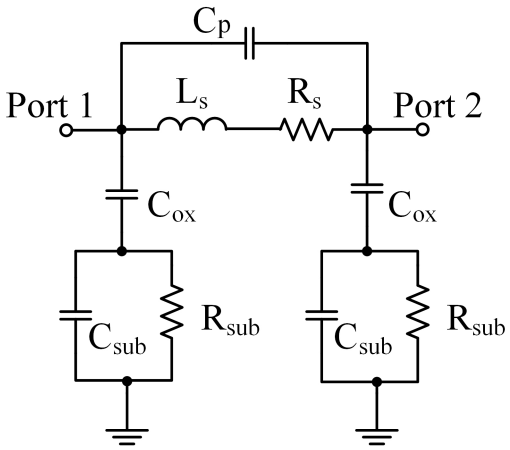


Figure 1.11: Typical integrated inductor physical model (π-model)

can be global or local. The former ones try to construct a high-fidelity model that is as accurate as possible over the complete search space. Once the model is built, it can be used as a fast performance evaluator in an optimization algorithm for inductor synthesis [56]. However, it has been reported that these models may be highly inaccurate in some regions of the design space, yielding suboptimal results [57]. On the contrary, local models are iteratively improved during the inductor optimization process [58]. An initial coarse model is first created by using a few electromagnetically simulated training points. Then, this coarse model is used within a population-based optimization algorithm and, at each iteration, promising solutions (typically one) are simulated electromagnetically. The data from these EM simulations are used to improve the accuracy of the surrogate model in the region where the new simulation points are added, while evolving towards the presumed optimal inductor. However, the results may highly depend on the accuracy of the initial coarse surrogate model. A prescreening technique, e.g., the expected improvement (EI) method, which can be used to increase the quality of the optimization process, consists in using the uncertainty measurement of the prediction, i.e., the mean square error (MSE), instead of just the predicted value to rank promising solutions. These methods have been widely applied to single-objective optimization [59, 60] and some more recent attempts have tried to extend these approaches to the multi-objective case [61–63].

1.3.3. Taking into Account Layout Parasitics

Nowadays, the circuit sizing automation by means of optimization-based techniques is an established concept. However, in order to achieve robust circuit designs, complete circuit layout parasitic effects have to be considered during the automatic flow. This is even more critical for RF ICs where the impact of the layout parasitics is highly destructive due to the high operating frequencies.

Parasitic-Inclusive Methodologies

During the past few years, several parasitic-inclusive methodologies were developed. These methodologies tried to shorten the gap between schematic and physical circuit implementations.

Parasitic-inclusive methodologies are approaches that use performance/symbolic models in order to estimate the impact of the layout parasitics and calculate the circuit performances. Some works, such as [64, 65], use symbolic models in order to estimate the effects of critical interconnections and layout parasitics. By using performance models, the layout parasitic estimation may sometimes be inaccurate. These approaches, based on performance models, are illustrated in Fig. 1.12 (a). In [66–68] the parasitics are extracted from a first coarse layout, and afterwards this parasitic information is used in order to create models which are then used during the optimization to estimate the performance of given solutions. The problem is that the parasitic information associated with a single layout design (or a reduced set) does not capture all parasitic variations that could be found during sizing, and, therefore, promising solutions may be lost. These approaches, based on parasitic sampling, are illustrated in Fig. 1.12 (b).

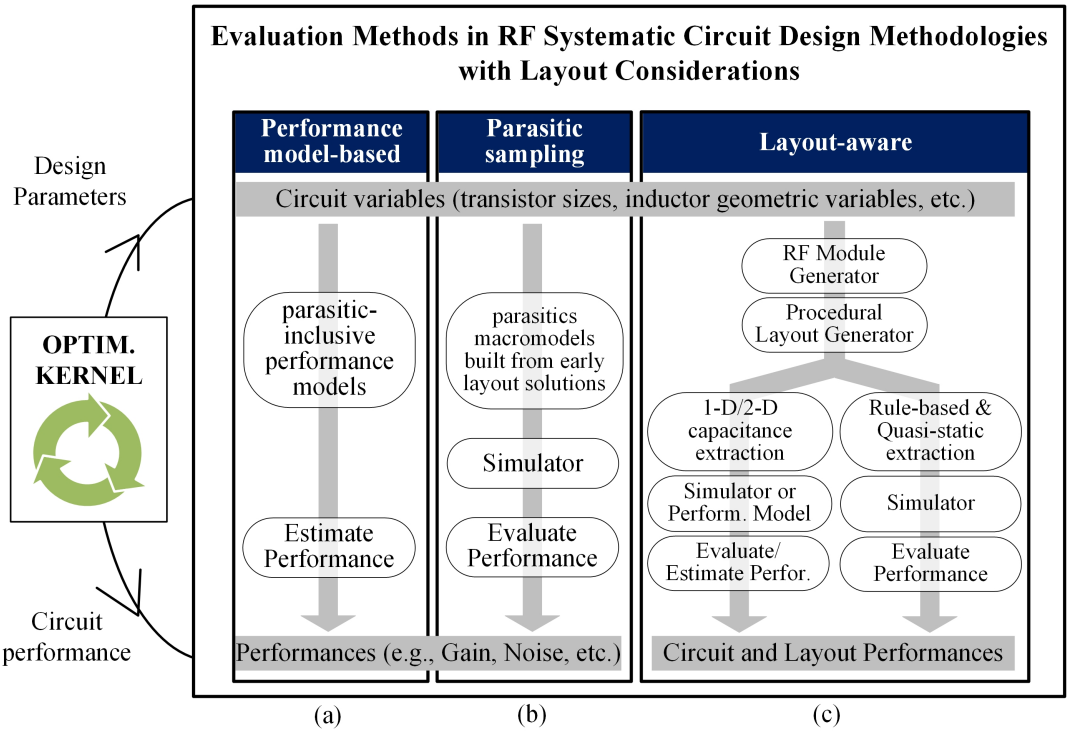


Figure 1.12: Illustrating different strategies to include parasitics in optimization-based methodologies.

None of the methodologies presented in Fig. 1.12 (a) and (b) perform an explicit layout generation during the optimization flow for each tentative sizing. The methodologies that are able to create a layout for each sizing solution during the optimization loop are designated as layout-aware methodologies, and are described in the following sub-Section

Layout-Aware Methodologies

While layout generation in-the-loop (Fig. 1.12 (c)) represents an overhead during optimization, having the layout readily available allows the computation of the precise parasitics for each specific solution without approximations.

In [69, 70] RF-specific methodologies were developed. In these works, a tool that is able to generate the physical layout of a device by means of an automatic routine is used. Such tool is defined as a module generator (MG) [71]. In [69], this MG was integrated into an automatic layout generator that uses automatic routines in order to place the devices in a previously described and always fixed position[2]. The tools that follow the same procedure/routine to perform the circuit layout are defined as procedural layout generators. Procedural generators are used to create the layout of each individual solution during the optimization, and while in [69] only the parasitics of the critical nets were extracted using 1D/2D capacitance models, in [70], a more extensive set of parasitics are obtained using standard rule-based and quasi-static inductance extraction techniques. These techniques are illustrated in Fig. 1.12 (c).

It can be concluded that the only RF-specific methodologies that perform an automatic layout during the optimization loop adopt limitative procedural layout generators. Therefore, in order to obtain a more dynamic approach, instead of the procedural layout generators, template-based approaches should be considered [72–75]. In these template-based approaches the designer defines a layout template (or multiple templates) for a given circuit which may include a complete description of the floorplan.

For parasitic extraction, the analytical/geometrical 1D/2D, rule-based and quasi-static methods present satisfactory results for baseband, however, the accuracy of such extractions is inferior when compared to the accuracy of 2.5D rule-based techniques or 3D field solvers. Therefore, for the upmost accuracy, these 2.5D rule-based techniques or a 3D field solver should be used.

1.3.4. Taking into Account Process Variability

When designing a circuit, the designer must take into account that some variation will occur between the simulated and the fabricated design. Variation is a huge problem in nanometer technologies, and failing to effectively take into account these variations can cause re-design iterations which ultimately result in product delays. These are serious issues that directly impact the revenues, profits, and ultimately, valuations of semiconductor companies and foundries alike. The variation causes may take many forms: environmental variations, such as temperature, power supply voltage, etc, or process and mismatch variations. While the environmental variations affect the circuit after its fabrication, process and mismatch variations are introduced during manufacturing, by random dopant fluctuations and other manufacturing problems (lithography, etc.). The process variations are inter-die, meaning that they affect all dies' equally. On the other hand, the mismatch is an intra-die phenomena, which means they affect devices in the same die. Several automatic design methodologies have been proposed, that incorporate the variability effects into their flow in different ways. Some approaches estimate the circuit performances at its performance "corners". A corner is a point in the performance variation space, which represents the (supposedly) bounds of the model parameters. These corners enable a fast strategy to include process variability in automatic design methodologies. However, by considering only the device

[2] e.g., device A placed left of device B, device C on top of device A and B.

corner performances, the designer does not have an insight on the mismatch and on an important measure in variability-aware methodologies: the yield. The yield is the percentage of manufactured circuits that meet specs across all environmental conditions, expressed as a percentage, such as e.g., 95% [76]. In order to have a yield estimation, the designer must perform a circuit statistical analysis, such as Monte-carlo. However, this analysis involve hundreds of simulations which is a very time-consuming process. This process gets even worse when optimization-based methodologies are used, where thousands of simulations would have to be performed. In [77], a variability-aware methodology is considered by calculating the circuit performances at the nominal and performance corners of each tentative sizing solution. By doing so, the designer guarantees that his/her design will work even in the most pessimistic situations. In [78], a tool for the automated variation-aware sizing of analog integrated circuits is presented. This tool allows nominal, environmental and process corner simulation in order to estimate the variability of the circuit. Furthermore, the tool uses response surface models in order to speed up the optimization. In [79], a method to calculate the trade-off between the yield and a figure of merit is presented. A quasi-Monte-carlo sampling is performed in order to calculate the yield in a more efficient way. In [80], a technique based on artificial intelligence is used in order to speed up the yield optimization. However, this solution is implemented using single-objective algorithms rather than multi-objective. In [81], an efficient yield optimization technique for multi-objective optimization-based automatic analog integrated circuit sizing is presented. The proposed yield estimation technique reduces the number of required Monte-carlo simulations by using the k-means clustering algorithm, with a variable number of clusters, to select only a handful of potential solutions where the Monte-carlo simulations are performed.

There is an efficiency/over-design trade-off between the available methodologies to consider the process variations. While considering performance corners is an efficient solution, performing Monte-carlo simulations is a more time consuming option. The trade-off appears because if the designer considers the performance corners, he/she may be over-designing the circuit. It should also be taken into account that by using corners the mismatch between devices is also not considered.

1.3.5. Circuit Complexity

In the previous Sections, the needs for an automated and efficient RF circuit design methodology were presented. However, it is important to discuss the circuit complexity that the methodology is able to cope with.

In the past, most efforts directed to system-level[3] design were focused in the direction of high-level system specification tools, RF budget analyzers and architecture comparison tools [33, 82–84]. These high-level tools are very handy in top-down design methodologies because they are used in order to estimate lower-level circuit performance in order to fulfill the complete system specifications. After specifying the needed performances for each circuit, and, following a top-down approach, the

[3]In this thesis we denote by *system* any set of two different circuits that are connected

designer starts from the higher level until reaching the lowest possible level (e.g., synthesizing the passive components). However, while going down the hierarchy, the designer may realize it may be difficult or even impossible to synthesize the needed performances for some circuit/passive, which ultimately will lead to unwanted re-design cycles. Also, these high-level tools do not consider all circuit nonlinearities and therefore it may be difficult to guarantee that the specifications given by the tool will be met at transistor-level, which again, can lead to re-design cycles. Eventually, since the high-level specifications do not entirely match the transistor specifications, the designer can choose to over-design the RF system in order to reduce the re-design cycles. However, this would ultimately lead to sub-optimal designs (e.g., circuits with higher power consumption). In [85], S. Rodriguez et al, created a tool that was able to automatically size each circuit of an RF system based on system specifications. In this work the entire system is optimized at once with no top-down or bottom-up hierarchy. By using an optimization engine, each component of each circuit composing the system would be automatically sized. However, the tool presents some drawbacks: the circuit performances are estimated using analytical equations during the optimization stage and ideal models are used for the passive components. By using analytical equations, the optimization is very efficient, however the circuit performances may change significantly from an actual electrical simulation. Hence, it is reported in the paper that a fine-tuning operation must be performed in order to meet the desired specifications after the optimization. One of these fine-tuning operations is portrayed, where some components had to be changed in more than 50% from its initial value. In [86], Z. Pan et al, build performance models for each circuit of an RF front-end receiver and a VerilogA description of these circuits is constructed in order to simulate the circuit performances. While for complex systems, such as, e.g., an RF transceiver, full system simulation is not practical to perform in an electrical simulator, for smaller systems such as a receiver, this simulation is still manageable. Therefore, electrical simulators should be preferred instead of performance models, in order to achieve superior accuracies. Thus, in [86], the system design is efficient but when the design is actually simulated at transistor-level, the performances are expected to change due to the usage of approximated performance models.

Optimizing the system entirely as in [85] is an inefficient solution because RF systems may be highly complex with a huge set of design variables and specifications, which can degrade the convergency of the optimization algorithm. On the other hand, using analytical equations and performance models as in [86], will inevitably lead to inaccurate designs. Therefore, it can be concluded that automating the design of an RF system and accurately estimate its performances is not a straightforward task. The scenery gets even more clear, because from the several works that use transistor-level simulations together with optimization-based methodologies for the automated design of RF circuits (e.g., [29, 30, 35, 40, 48, 49, 65, 87–89]) only M. Chu in [89] connected an LNA and a mixer. This fact is due to the high amount of design variables, circuit/system specifications and the difficulties to efficiently calculate the system performances.

1.4. Innovative Contributions

After pointing out the needs for an accurate and efficient RF automated circuit design methodology in the previous Section, a list of the innovative contributions proposed in this thesis is given here. The objective of these contributions is to help solving some of the issues previously described.

- **Development of a state-of-the-art surrogate model for integrated inductors.** In this thesis, in order to accurately model integrated inductors, a surrogate model was developed that has less than 1% error when compared to EM simulations, while reducing the simulation time by three orders of magnitude. Several different models were created for different inductor topologies, all of them achieving negligible errors when compared to EM simulations.

- **Integrated inductor synthesis using different strategies and optimization algorithms.** Due to the accurate and efficient surrogate model developed, its usage in optimization methodologies is very practical. Several different inductor synthesis strategies were applied and compared. Furthermore, a state-of-the-art tool, SIDe-O, was created. SIDe-O is a computer-aided design tool developed for the design and optimization of integrated inductors based on surrogate modeling techniques and the usage of evolutionary optimization algorithms. Furthermore, the tool allows the creation of S-parameter files that accurately describe the behavior of inductors for a given range of frequencies, which can later be used in SPICE-like simulators for circuit design in commercial environments. The surrogate models developed, and integrated in the tool, provide a solution to the problem of accurately and efficiently modeling and optimizing inductors, which alleviates the bottleneck that these devices represent in the RF circuit design process

- **RF bottom-up circuit design methodology using efficient strategies.** In this thesis, bottom-up design methodologies are applied to the design of RF circuits, starting at the lowest possible level: passive component level. The methodology uses the developed SIDe-O tool in order to generate inductor POFs, which can later be used in circuit simulations. Furthermore, several different simulation strategies are used in order to reduce the circuit simulation time. By using such strategies some of the most expensive RF performances (e.g., third-order intercept point) can be efficiently calculated and considered during the automated design of RF circuits.

- **Development of a specific RF layout-aware methodology.** A layout-aware methodology was developed especially for the design of RF circuits. The methodology uses a multi-objective optimization algorithm and a bottom-up design methodology. An automatic layout generation is carried in-the-loop for each tentative sizing solution using a state-of-the-art MG, template-based placer and router, which were specifically developed for RF circuits. The proposed approach exploits the full capabilities of most established computer-aided design tools for RF design available nowadays, such as the RF circuit simulator as performance evaluator and commercial

layout parasitic extractor to determine the complete circuit layout parasitics. Furthermore, the inductor parasitics are considered using the previously developed surrogate model.

- **Taking into account process variability in automated design methodologies.** The methodology developed, allows the user to consider the corner extreme performances during not only the sizing optimization, but also during the layout-aware optimization, increasing therefore the design robustness.
- **Multilevel RF bottom-up circuit design with transistor-level accuracy.** Also, in this thesis an automatic multilevel bottom-up strategy is developed. By using such multilevel bottom-up strategy different circuits can be connected in order to build an RF system. Furthermore, each level of the hierarchy is simulated with the upmost accuracy possible: EM accuracy at passive level, and electrical simulations at circuit/system level. Moreover, the methodology encourages the hierarchical POF reuse. The methodology presented in the thesis is the first to present such multilevel bottom-up optimizations, and therefore being able to design RF systems.

1.4.1. Thesis Organization

In order to show the innovative contributions in practice, the methodology developed in the thesis will be applied to the design of different RF circuits with the final objective of designing an RF front-end receiver. The thesis will be centered around three typical RF circuits: the low noise amplifier (LNA), the voltage controlled oscillator (VCO) and the mixer.

Since the final objective of this thesis it to design an RF front-end receiver, it is important that the traditional receiver architectures are briefly reviewed. Therefore, this is performed in Chapter 2. Furthermore, in the same Chapter the three main blocks that constitute the RF front-end (LNA, VCO and mixer) are also described, as well as its most important performance parameters.

In chapter 3, the new modeling strategy for the accurate design of integrated inductors is presented. Afterwards, the model is used in order to synthesize integrated inductors using several different strategies. Furthermore, the developed models were integrated into a novel tool that is able to assist designers into modeling and optimization of inductors [Journal 1 and 2 of Section 1.5.1 and Conf. 1 to 4 of Section 1.5.2].

In Chapter 4, the advantages of using an accurate inductor modeling in optimization-based strategies are presented for the specific case of an LNA design [Journal 3 of Section 1.5.1]. Also, in Chapter 4, the bottom-up methodologies are used to design the LNA and two different strategies to design passive components in optimization-based methodologies are compared against over an extensive statistical study, also considering an LNA case study [Journal 4 of Section 1.5.1]. Furthermore, in the same Chapter, a VCO is designed using a corner-aware bottom-up design

methodology, and the importance of considering this extreme device performances in a first design stage is illustrated [Journal 5 of Section 1.5.1]. The synthesis of a Gilbert cell mixer is also performed in Chapter 4, in order to present all the circuits necessary to design the RF front-end receiver.

Chapter 5 presents a methodology where a layout-aware optimization is described and used for the design of a VCO and a LNA [Journal 6 of Section 1.5.1 and Conf. 6 and 7 of Section 1.5.2]. Also, in Chapter 5, the previously presented layout-aware methodology is further elaborated in order to take into account device process variability to develop a layout-corner-aware optimization. This methodology is then used to design a VCO as case study.

Chapter 6 presents the bottom-up automated design of a complete RF front-end with transistor-level accuracy. Furthermore, a comparison is performed between three different optimization strategies applied to a system level [Journal 7 of Section 1.5.1].

In the end, Chapter 7 draws conclusions and present some future work ideas.

1.5. Publications and Achievements

1.5.1. Journals

1. F. Passos, E. Roca, R. Castro-López, F.V. Fernández, "Radio-frequency inductor synthesis using evolutionary computation and Gaussian-process surrogate modeling", Applied Soft Computing, Volume 60, 2017, Pages 495-507, ISSN 1568-4946, http://dx.doi.org/10.1016/j.asoc.2017.07.036.

2. F. Passos, E. Roca, R. Castro-López, F.V. Fernández, "An inductor modeling and optimization toolbox for RF circuit design", in Integration, the VLSI Journal, Available online, 27 January 2017, ISSN 0167-9260. https://doi.org/10.1016/j.vlsi.2017.01.009.

3. F. Passos, R. González-Echevarría, E. Roca, R. Castro-López, F.V. Fernández, "A two-step surrogate modeling strategy for single-objective and multi-objective optimization of radiofrequency circuits", in Soft Computing, currently in second round of review process.

4. F. Passos, E. Roca, R. Castro-López, F.V. Fernández, "Automated RF circuit design methodologies: online vs. offline passive component design", in IEEE Transactions on VLSI, currently in review process.

5. F. Passos, R. Martins, N. Lourenço, R. Póvoa, A. Canelas, E. Roca, R. Castro-López, F. V. Fernández, N. Horta, "Enhanced Systematic Design of a Voltage Controlled Oscillator using a Two-Step Optimization Methodology", in Integration, the VLSI Journal, currently in second round of review process.

6. R. Martins, N. Lourenço, F. Passos, R. Póvoa, A. Canelas, E. Roca, R. Castro-López, F. V. Fernández, N. Horta, "Two-Step RF IC Block Synthesis with Pre-optimized inductors and Full Layout Generation In-the-loop", in IEEE Transactions on Computer-aided design of circuits and systems, currently in second round of review process.

7. F. Passos, E. Roca, J. Sieiro, R. Fiorelli, R. Castro-López, J. M. López-Villegas, F. V. Fernández, "An Efficient Synthesis Strategy for RF Systems Based on Bottom-up Design Methodologies and Hierarchical Reusability", in IEEE Transactions on Computer-aided design of circuits and systems, currently in review process.

1.5.2. Conferences

1. F. Passos et al., "Physical vs. surrogate models of passive RF devices," 2015 IEEE International Symposium on Circuits and Systems (ISCAS), Lisbon, 2015, pp. 117-120. doi: 10.1109/ISCAS.2015.7168584

2. F. Passos, R. González-Echevarría, E. Roca, R. Castro-López and F. V. Fernández, "Surrogate modeling and optimization of inductor performances using Kriging functions," 2015 International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Istanbul, 2015, pp. 1-4. doi: 10.1109/SMACD.2015.7301675

3. F. Passos, R. González-Echevarría, E. Roca, R. Castro-López, and F. V. Fernández. 2016, "Accurate synthesis of integrated RF passive components using surrogate models", in Proceedings of the 2016 Conference on Design, Automation & Test in Europe (DATE '16), pp. 397-402, Dresden, 2016.

4. F. Passos, E. Roca, R. Castro-López and F. V. Fernández, "SIDe-O: A toolbox for surrogate inductor design and optimization," 2016 13th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Lisbon, 2016, pp. 1-4. doi: 10.1109/SMACD.2016.7520713

5. F. Passos, E. Roca, R. Castro-López, F. V. Fernández, J. Sieiro and J. M. López-Villegas, "A strategy to efficiently include electromagnetic simulations in optimization-based RF circuit design methodologies," 2017 IEEE MTT-S International Conference on Numerical Electromagnetic and Multiphysics Modeling and Optimization for RF, Microwave, and Terahertz Applications (NEMO), Seville, 2017, pp. 64-66. doi: 10.1109/NEMO.2017.7964188

6. R. Martins et al., "Layout-aware challenges and a solution for the automatic synthesis of radio-frequency IC blocks," 2017 14th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Giardini Naxos, 2017, pp. 1-4. doi: 10.1109/SMACD.2017.7981577

7. F. Passos et al., "Systematic design of a voltage controlled oscillator using a layout-aware approach," 2017 14th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Giardini Naxos, 2017, pp. 1-4. doi: 10.1109/SMACD.2017.7981580

1.5.3. Journals not included in this thesis

1. F. Passos, Y. Ye, D. Spina, E. Roca, R. Castro-López, T. Dhaene, F.V. Fernández, "Parametric macromodeling of integrated inductors for RF circuit design", in Microwave and Optical Technology Letters, Vol. 59, issue 5, pp. 1207-1212, May 2017.

1.5.4. Conferences not included in this thesis

1. F. Passos et al., "Frequency-dependent parameterized macromodeling of integrated inductors," 2016 13th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Lisbon, 2016, pp. 1-4. doi: 10.1109/SMACD.2016.7520750

2. N. Lourenço et al., "New mapping strategies for pre-optimized inductor sets in bottom-up RF IC sizing optimization," 2017 14th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design (SMACD), Giardini Naxos, 2017, pp. 1-4. doi: 10.1109/SMACD.2017.7981582

3. F. Passos, E. Roca, R. Castro-López and F. V. Fernández, "An algorithm for a class of real-life multi-objective optimization problems with a sweeping objective," 2017 IEEE Congress on Evolutionary Computation (CEC), San Sebastian, 2017, pp. 734-740. doi: 10.1109/CEC.2017.7969383

1.5.5. Achievements

1. Electronic Design Automation (EDA) competition winner in SMACD 2016

2. Nominee for the Best Paper Award in SMACD 2017

2

RF Receiver Architectures

The objective of a communication system is to send information from a transmitter to a receiver. Therefore, the transmitter has to be appropriately designed in order to send signals with adequate power levels, and the receiver has to be able to receive a signal and extract the message. In this thesis we will focus on the receiver part of the communication chain. Therefore, this chapter will present a brief overview of this system, providing the main performances and parameters for each block included.

The goal of any radio receiver is to extract and detect selectively a desired signal from the complete electromagnetic spectrum. The ability to select a given signal in the presence of the huge amount of interfering signals and noise is the fundamental task for radio receivers. Nowadays, radio receivers must often be able to detect signal powers as small as a few nano-watts, while rejecting a multitude of other signals that may be several orders of magnitude larger [90]. Because the electromagnetic spectrum is a limited resource, interfering signals often lie very close to the desired signal, thereby increasing the difficulty of rejecting the unwanted signals. Over the times, several different receiver architectures were proposed, each one with its pros and cons. Since in this thesis the final objective is to achieve the design of an RF front-end, it is important to review the different available receiver architectures. Hence, in Section 2.1 a brief description of some of the most common radio architectures used is performed. Afterwards, in Section 2.2, the blocks that constitute the RF front-end, and that will be designed throughout this thesis are reviewed. Their main purpose to the receiver chain is discussed and their most important performance parameters are examined.

2.1. Receiver Architectures

2.1.1. Superheterodyne Receiver

The superheterodyne receiver architecture was the dominant choice for many decades [91]. Its generic architecture is shown in Fig. 2.1.

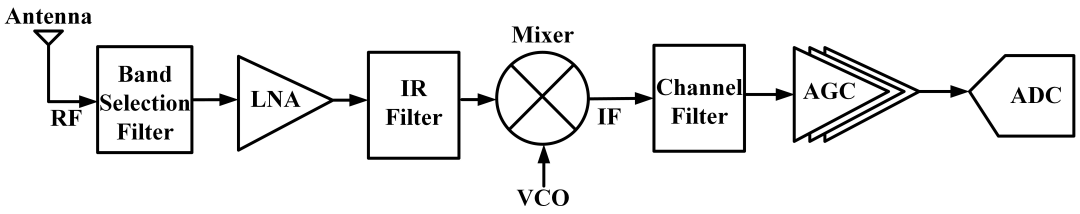


Figure 2.1: Typical superheterodyne integrated RF receiver signal chain.

The superheterodyne features a band-selection filter between the antenna and the LNA, which rejects the out-of-band interference. Then, the signal is amplified by an LNA which is then followed by an image-rejection filter. This filter has the purpose of rejecting the unwanted image frequency band (which will be explained later). A mixer then converts the RF signal to a lower-frequency, which is commonly referred to as intermediate frequency (IF). Both the RF signal and a local oscillator (LO) signal (which can be generated by a VCO) enter the mixer, thereby generating the IF signal that appears at the mixers' output. The frequency of this IF signal is equal to the difference between the RF input signal frequency and the LO signal frequency. Therefore, the channel selection is performed by changing the oscillation frequency of the VCO. After the frequency down-conversion operation, a channel filter is implemented in the IF stage to remove any unwanted signals. Next, an automatic gain control (AGC) amplifier provides a significant amount of gain to the IF signal. The amplified IF signal is then demodulated, allowing the information to be processed. This architecture is known for being able to select narrow band signals from an environment full of interferers [92]. Since the channel selection is carried out at IF the dynamic range requirements are relaxed at baseband, which simplifies the design of the ADC [91].

One of the disadvantages of superheterodyne receivers is the image problem [92]. To understand this issue, note that an analog multiplier does not preserve the polarity of the difference between two signals, i.e., for $x_1(t) = A_1 cos(\omega_1 t)$ and $x_2(t) = A_2 cos(\omega_2 t)$, the product of $x_1(t)$ and $x_2(t)$ signals is cos$[(\omega_1 - \omega_2)t]$, which is not different from cos$[(\omega_2 - \omega_1)t]$. Therefore, in the superheterodyne architecture, the bands symmetrically located above and below the LO frequency are down-converted to the same center frequency at IF (see Fig. 2.2). If the band of interest is f_1, then the image is around $2f_{LO} - f_1$ and vice versa. Due to this problem, the noise present at the image band is also translated into the desired band.

Therefore, the total noise at IF is composed by the noise at the desired RF band, down-converted to IF, plus the noise at the image RF band up-converted to IF and also the noise added by the mixer

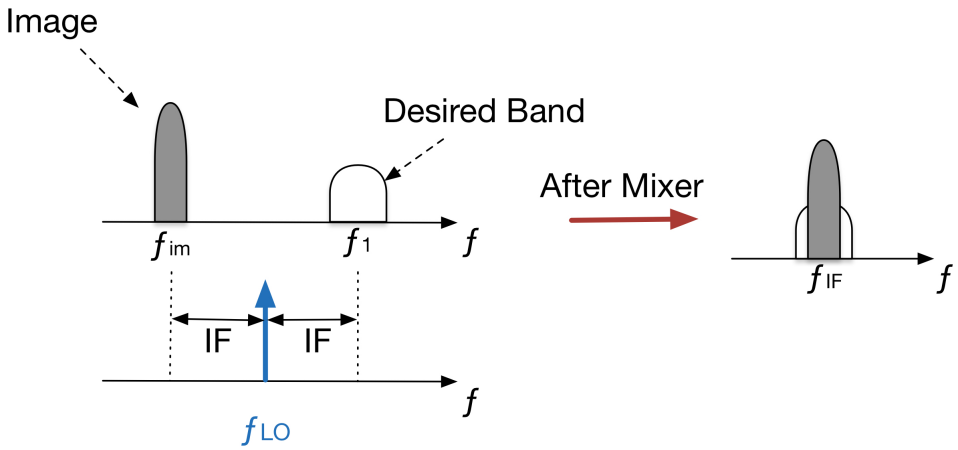


Figure 2.2: Illustrating the image problem in superheretodyne receivers.

circuit itself. Therefore, in this type of architecture, high quality factor filtering is usually required in order to meet the specifications of the communication standards. In order to design such high quality factor filters, the image rejection (IR) filter and/or the channel selection IF filter have to be implemented off-chip. Also, different image rejection and channel selection filters have to be used for different standards, making it difficult to achieve a highly integrated low cost solution [83]. Therefore, this receiver is not particularly suited for IC design.

2.1.2. Zero-IF Receiver

A receiver with its IF set to zero is called zero-IF, direct conversion or homodyne receiver. The architecture of this type of receiver is shown in Fig. 2.3.

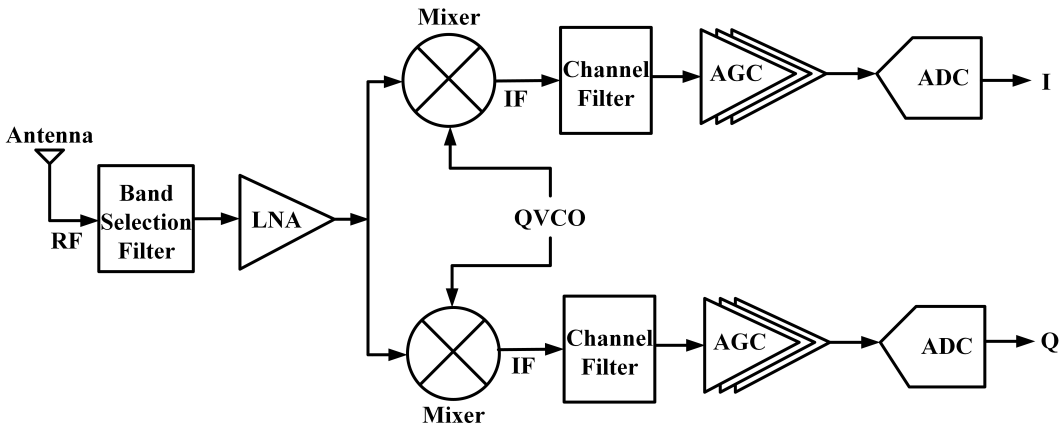


Figure 2.3: Typical zero-IF integrated RF receiver signal chain.

It can be seen in Fig. 2.3, that a Quadrature-VCO (QVCO) drives two different mixers. The QVCO generates two different signals with opposite phases which then drive two different mixers. It is shown in [92] that the signals at the output of the mixers have the same polarity, containing its

images at opposite polarity [92]. Thus, in the ideal case, the sum of the two output signals is an image-free signal. This is the main advantage of zero-IF receivers. Therefore, this architecture is more suitable for integration than the standard superheterodyne receiver because no IR filter is needed.

However, some disadvantages outcome from the use of this architecture. The main disadvantage of these receivers is the appearance of a DC offset at the mixer output. Since in this architecture the down-converted band is at zero frequency, inappropriate offset voltages can corrupt the signal and saturate the following stages. The causes for the DC offset can be observed in Fig. 2.4. The first cause for DC offset is the so-called LO leakage. This phenomena appears due to capacitive and substrate coupling. The signal from the LO now appears at the input of the LNA and the mixer signal is *mixed* with this signal. This phenomena is sometimes called "self-mixing" [92]. A similar effect occurs if a large signal interferer leaks from the LNA to the LO and is multiplied by itself.

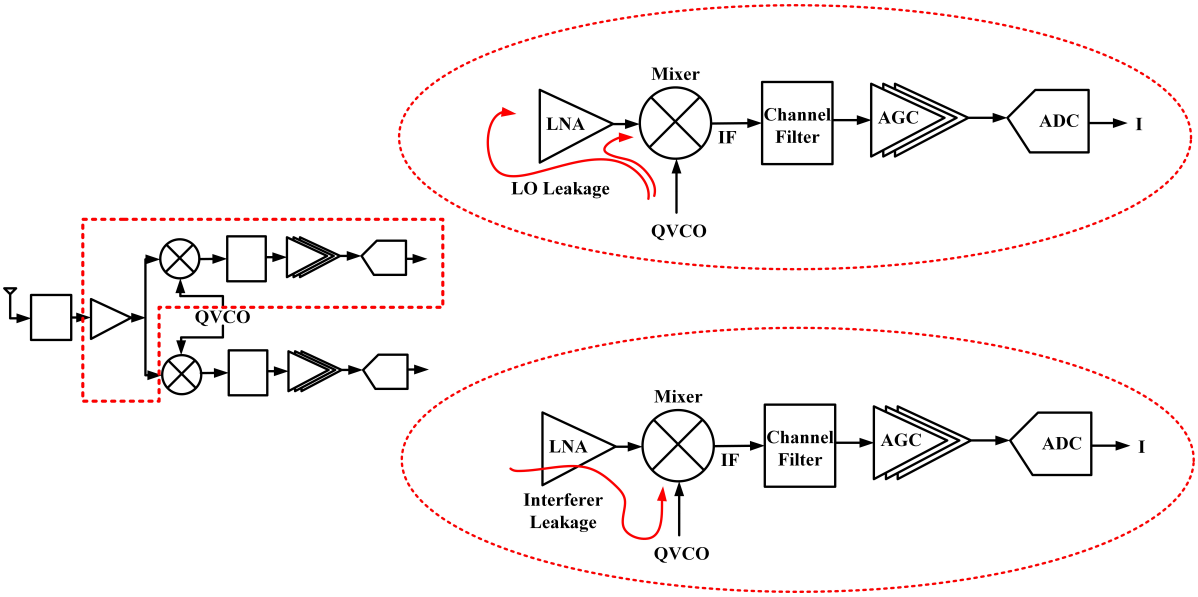


Figure 2.4: Self mixing of the LO signal and a strong interferer.

Another problem of zero-IF architectures is the Flicker noise. Flicker noise (sometimes also referred to as $1/f$ noise) appears in MOS transistors when these are operating near the zero frequency range. This noise is usually generated when a direct current flows through the MOS transistors. Since in zero-IF receivers we are translating the signal to zero frequency, this noise usually highly affects this type of receivers.

2.1.3. Low-IF Receiver

The low-IF receiver architecture has a block diagram similar to the zero-IF one shown in Fig. 2.3. Low-IF receivers perform frequency down-conversion of the signal to frequencies close to, but higher than zero. This architecture presents a trade-off between the superheterodyne and the zero-IF

receivers. If in one hand, the DC offset and Flicker noise problems of the zero-IF receivers are solved, on the other, hand the image problem is back and this time with the additional difficulty of filtering it at a very low frequency.

There are several other receiver architectures available in literature [91, 93]. Depending on the application, each architecture presents its pros and cons, and the designer must chose it intelligently and carefully. In the next Section, the receiver blocks that constitute the front-end receivers are briefly described, as well as its main performances parameters.

2.2. Front-End Receiver Blocks

The three main blocks of the front-end receiver, which are the common to all receiver architectures are: the LNA, the VCO and the mixer. In this Section these blocks are introduced and their most important performances are described. Nevertheless, there are two main performances that are common not only to these three blocks but to all CMOS circuits in general, which are the power consumption and the area occupation.

Power Consumption

Power is very important in RF circuit design. Nowadays, in an era where all devices aim at portability and at continuous interconnection (e.g., IoT), the battery of a given device is very important. Therefore, power consumption has to be kept at a minimum. It is possible to understand that higher power dissipation limits a circuit because portable electronic devices are limited by battery life. Therefore, power is one of the most important system performance metrics. When we speak about the power consumption of a circuit we are usually interested in the DC power consumption given by,

$$P_{DC} = V_{DD} \cdot I_{DC} \tag{2.1}$$

where V_{DD} is the power supply voltage and I_{DC} is the total DC current of the circuit. Therefore, if the designer wishes to minimize the power consumption, he/she can reduce power supply levels or reduce the current level, or if possible, reduce both.

Area Occupation

The area in CMOS integrated circuits is directly associated with cost because larger area reduces the number of dies that can fit into a wafer and therefore leads to a linear increase in processing and material costs. Another significant issue, is the impact of die area on die yield. It has been reported that the yield (the fraction of the fabricated ICs that are fully functional) decreases sharply with die area. As a result, die manufacturing costs quickly become prohibitive beyond some size determined by the process technology, not only by the cost associated with area, but also due to the yield of a given die [94].

2.2.1. Low Noise Amplifier

An LNA is an electronic circuit whose objective is to amplify a very low-power signal without significantly degrading its signal-to-noise (SNR) ratio. The SNR is a measure used to compare the level of a desired signal strength to the level of noise (see Fig. 2.5).

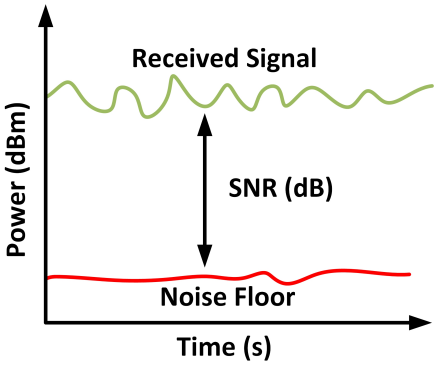


Figure 2.5: Illustrating the SNR.

The LNA symbol is shown in Fig. 2.6. The LNA is usually one of the first components just after the antenna in an integrated wireless receiver chain. The weak signal received at the antenna is fed into the LNA. In order to absorb as much signal power as possible from the antenna, the LNA needs to provide a sufficiently matched input impedance. Being one of the first elements in the receiver chain the LNA is a key block for the noise performance of the whole chip.

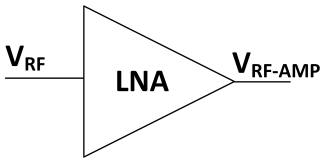


Figure 2.6: Low noise amplifier symbol.

The LNA can be considered as a two-port system and, therefore, it is important to establish the concept of Scattering Parameters, or S-Parameters for short. The S-parameters describe the response of an N-port network to incident signals, to any or all of the ports. Consider the two-port network illustrated in Fig. 2.7.

The signal at each of the ports, can be thought of as the superposition of two waves traveling in

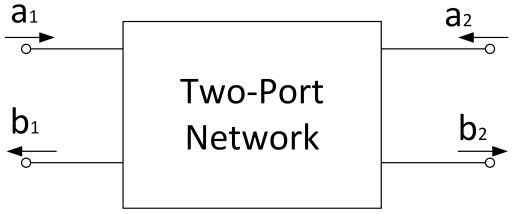


Figure 2.7: Two-port network.

opposite directions (e.g., a_1 and b_1). By convention, each port is shown as two nodes in order to give a name and value to these opposite direction waves. The variable a_i represents a wave incident to port i and the variable b_j represent a wave reflected from port j. The magnitude of the a_i and b_j variables can be thought of as voltage-like variables, normalized using a specified reference impedance (e.g., Z_0). The S-parameters can be defined as,

$$\begin{aligned} S_{11} &= \frac{b_1}{a_1} \\ S_{12} &= \frac{b_1}{a_2} \\ S_{21} &= \frac{b_2}{a_1} \\ S_{22} &= \frac{b_2}{a_2} \end{aligned} \tag{2.2}$$

where S_{11} is the input reflection coefficient, S_{22} the output reflection coefficient, S_{21} the forward transmission coefficient and S_{12} is the reverse forward transmission coefficient. The first number in the S-Parameter subscript refers to the responding port, while the second number refers to the incident port. Hence, S_{21} means the response at port 2 due to a signal at port 1. These S-parameter are important for the understanding of the LNA performance parameters, which are described below.

Gain

The gain is one of the most important performance measures of LNAs. The gain quantifies the ability of a system to increase the amplitude of an input signal and in LNAs it is given by the forward transmission coefficient, S_{21}.

Noise Figure

Noise figure (NF) is a measure of degradation of the signal-to-noise (SNR) ratio in a given circuit. The NF can be defined as,

$$\text{NF} = 10 \cdot log_{10}\left(\frac{SNR_{in}}{SNR_{out}}\right) \tag{2.3}$$

where SNR_{in} and SNR_{out} are the signal-to-noise ratio measured at the input and output of the circuit, respectively.

Linearity

The basic idea for the calculation of non-linear effects is that the behavior of a circuit can be approximated by a non-linear equation:

$$y(t) = a_1 \cdot x(t) + a_2 \cdot x2(t) + a_3 \cdot x^3(t) + \ldots \tag{2.4}$$

where

- $y(t)$ is the output signal
- $x(t)$ is the input signal

- $a_1 > 0$
- $a_2 > 0$
- $a_3 < 0$.

If the circuit is considered ideally balanced, then the even order components are set to zero e.g., $a_2 = 0$ for convenience. When the input signal is a single-tone $x(t) = A \cdot cos(\omega_0 t)$, the generated output signal $y(t)$ consists of different frequency components:

$$\begin{aligned} y(t) = & \frac{1}{2}a_2A^2 \quad // \quad \text{corresponds to } dc \text{ component} \\ & + (a_1A + \frac{3}{4}a_3A^3)cos(\omega_0 t) \quad // \quad \text{corresponds to } \omega_0 \text{ component} \\ & + \frac{1}{2}a_2A^2cos(2\omega_0 t) \quad // \quad \text{corresponds to } 2\omega_0 \text{ component} \\ & + \frac{1}{4}a_3A^3cos(3\omega_0 t) \quad // \quad \text{corresponds to } 3\omega_0 \text{ component} \\ & + \dots \end{aligned} \tag{2.5}$$

Besides the emerging spectral components, it is worth noting that the linear amplification of the output fundamental is no longer a_1 but $(a_1 + \frac{3}{4}a_3A^2)$. This means that the third-order non-linearity reduces the voltage gain of the fundamental sine wave. The phenomenon is well known in literature and commonly characterized by the 1 dB compression point (CP_1) [92]. The CP_1 is defined as the power (or voltage) level for which the amplification of the fundamental frequency is attenuated by 1 dB compared to its ideal linear amplification a_1. From (2.5) it can be shown that for

$$A_{1dB} = \sqrt{0.145|a_1/a_3|} \tag{2.6}$$

the input referred 1 dB compression point (CP_{1i}) is reached.

Let us assume an input signal consisting of two fundamental tones $\omega = \omega_1$ and $\omega = \omega_2$ with different amplitudes A_1 and A_2:

$$x(t) = A_1 \cdot cos(\omega_1 t) + A_2 \cdot cos(\omega_2 t) \tag{2.7}$$

The output signal $y(t)$ results in

$$\begin{aligned} y(t) = {} & \frac{a_2}{2}(A_1^2 + A_2^2) \quad // \quad \text{corresponds to } dc \text{ component} \\ & + (a_1 + a_3(\frac{3}{4}A_1^2 + \frac{3}{2}A_2^2))A_1 cos(\omega_1 t) \quad // \quad \text{corresponds to } \omega_1 \text{ component} \\ & + (a_1 + a_3(\frac{3}{4}A_2^2 + \frac{3}{2}A_1^2))A_2 cos(\omega_2 t) \quad // \quad \text{corresponds to } \omega_2 \text{ component} \\ & + \frac{a_2}{2}A_1^2 cos(2\omega_1 t) \quad // \quad \text{corresponds to } 2\omega_1 \text{ component} \\ & + \frac{a_2}{2}A_2^2 cos(2\omega_2 t) \quad // \quad \text{corresponds to } 2\omega_2 \text{ component} \\ & + a_2 A_1 A_2 cos((\omega_1 + \omega_2)t) \quad // \quad \text{corresponds to } \omega_1 + \omega_2 \text{ component} \\ & + a_2 A_1 A_2 cos((\omega_1 - \omega_2)t) \quad // \quad \text{corresponds to } \omega_1 - \omega_2 \text{ component} \\ & + \frac{a_3}{4}A_1^3 cos(3\omega_1 t) \quad // \quad \text{corresponds to } 3\omega_1 \text{ component} \\ & + \frac{a_3}{4}A_2^3 cos(3\omega_2 t) \quad // \quad \text{corresponds to } 3\omega_2 \text{ component} \\ & + \frac{3}{4}a_3 A_1^2 A_2 cos((2\omega_1 + \omega_2)t) \quad // \quad \text{corresponds to } 2\omega_1 + \omega_2 \text{ component} \\ & + \frac{3}{4}a_3 A_1 A_2^2 cos((\omega_1 + 2\omega_2)t) \quad // \quad \text{corresponds to } \omega_1 + 2\omega_2 \text{ component} \\ & + \frac{3}{4}a_3 A_1^2 A_2 cos((2\omega_1 - \omega_2)t) \quad // \quad \text{corresponds to } 2\omega_1 - \omega_2 \text{ component} \\ & + \frac{3}{4}a_3 A_1 A_2^2 cos((2\omega_2 - \omega_1)t) \quad // \quad \text{corresponds to } 2\omega_2 - \omega_1 \text{ component} \\ & + \dots \end{aligned} \tag{2.8}$$

First, let us assume that the input signals significantly differ in amplitude, i.e., $A_2 \gg A_1$. From (2.8) we see that the gain for the fundamental tone ω_2 will be reduced (desensitization) or may even drop to zero (blocking) [92]. If we assume that the second tone in (2.5) is modulated in amplitude by a sinusoid with $\omega = \omega_M$ e.g., $A_2(1 + mcos(\omega_M t))$, where $m < 1$ is the modulation index and $A_2 \gg A_1$, (2.8) changes into,

$$y(t) = [a_1 + \frac{2}{3}a_3 A_2^2(1 + \frac{m^2}{2} + \frac{m^2}{2}cos(2\omega_M t) + 2mcos(\omega_M t))]A_1 cos(\omega_1 t) + \dots \tag{2.9}$$

The gain for the signal at $\omega = \omega_1$ now contains amplitude modulation with $\omega = \omega_M$ and $\omega = 2\omega_M$. This phenomenon is called cross modulation [92]. Another interesting scenario is the presence of spectral components at $\omega = 2\omega_1 - \omega_2$ or $\omega = 2\omega_2 - \omega_1$ in the output signal $y(t)$ in (2.8). In Fig. 2.8, it is possible to observe two interferers at $\omega = \omega_1$ and $\omega = \omega_2$, which are located close to the wanted channel. The third-order intermodulation product at $\omega = 2\omega_2 - \omega_1$ falls into the wanted channel.

Assume two strong interferers with amplitudes A_1 and A_2 with a frequency spacing $\Delta\omega = \omega_2 - \omega_1$ so that the third-order intermodulation product occurring at $\omega = 2\omega_2 - \omega_1$ falls into a wanted frequency channel. If the wanted signal is too weak, the intermodulation product may dominate the spectra of the channel. Due to its position on the frequency axis, the intermodulation product cannot be filtered out. Literature commonly describes the effects of third-order intermodulation in terms of the third-order intercept point (IIP_3) (see Fig. 2.9). From (2.8) we see that the spectral power of the third-order

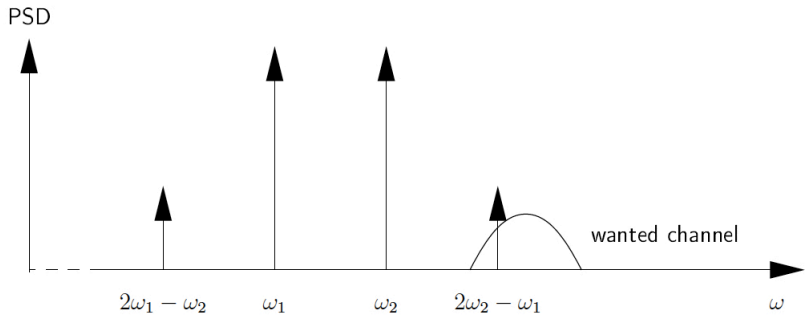


Figure 2.8: Illustrating the third-order intermodulation product at $\omega = 2\omega_2 - \omega_1$, which falls into the wanted channel [92].

products grows with the power of three while the fundamental components grow linearly. If we plot the output power P_{OUT} for the fundamental component and the third-order component versus the input power P_{IN} of the fundamental input tone of a non-linear circuit in logarithmic scale, it is possible to observe that the slope of the fundamental output tone is one while the slope of the third-order component is three (for small input powers far from the power levels where the circuit is already in compression). The parameter IIP_3 is commonly defined as the intersection of both lines.

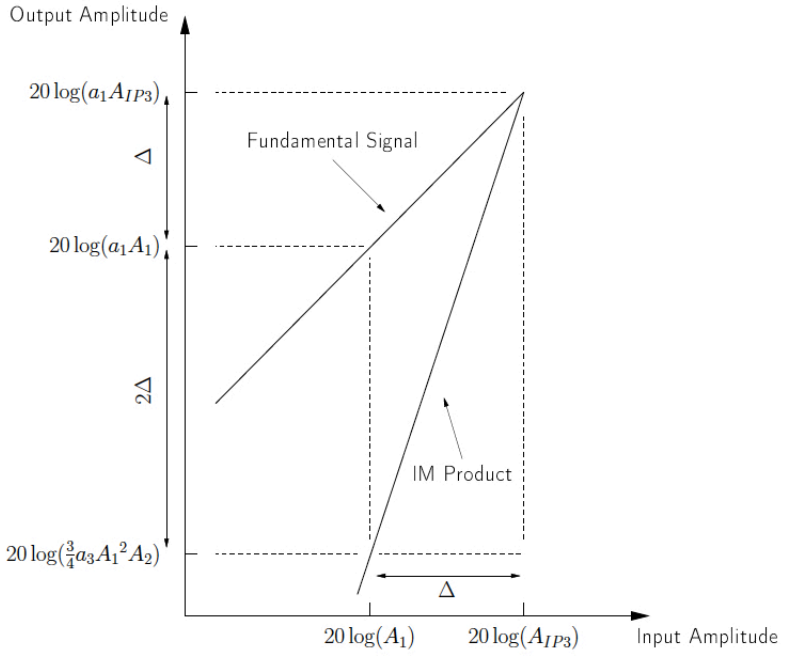


Figure 2.9: Graphical interpretation of the IIP_3 in double logarithmic scaling. The intermodulation product is growing with the power of three while the fundamental signal is growing linearly [92].

Input and Output Matching

The input and output matching are given by S_{11} (input matching), and S_{22} (output matching). When a circuit is connected to another, usually the input and output impedance do not entirely match. This means that part of the signal is not passed between circuits and is reflected back, loosing efficiency in the process. This is especially important for the LNA, since its input is connected to the antenna.

The antenna usually has a characteristic impedance of 50Ω and since the LNA is intended to capture a weak signal, the receiver can not afford to lose even more power, so the LNA must be carefully design to match the antenna impedance.

However, while it is absolutely necessary to take care of input impedance matching for the LNA, where the incident and reflected power in the circuit really exists, in some specific cases of IC design, the designer does not need to have perfectly matched circuits since in an IC circuit the size of the die is so small that the incident and reflective power or voltage waves are redundant or meaningless [95].

Stability

When discussing amplifiers, stability refers to an amplifiers' immunity to oscillation. Stability can be conditional or unconditional. Conditional stability means that the design is stable at certain input/output impedances, however, there is a region, of either source or load impedances, that can cause the circuit to oscillate. Unconditional stability refers to a network that can "see" any possible impedance and the design will not oscillate.

In order to evaluate the LNA stability, the Rollet's stability factor, K, can be used. This can be calculated from the S-parameters of the LNA as follows:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}||S_{21}|} \tag{2.10}$$

Port-to-Port isolation

The port-to-port isolation is a measure of how well the input and output of the LNA is separated in terms of unwanted signal coupling. For the LNA this performance is given by S_{12}, the reverse forward transmission coefficient.

2.2.2. Voltage Controlled Oscillator

The VCO is a circuit whose oscillation frequency is controlled by an input voltage, referred to as tuning voltage. By changing this voltage, the oscillation frequency shifts, therefore, the VCO is used in receivers in order to e.g., tune into a communication channel. The VCO is usually illustrated with the symbol shown in Fig. 2.10

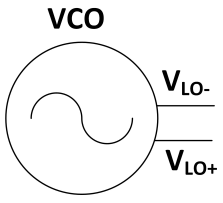


Figure 2.10: Voltage controlled oscillator symbol.

The most important performance parameters in VCO designs are given below.

Oscillation frequency

It is easy to understand that when discussing VCOs one of the most important parameters is the oscillation frequency, f_{osc}, which is the signal frequency generated at the output of the VCO.

Phase Noise

The phase noise, PN, is one of the main metrics of an oscillator in RF applications. In Fig. 2.11a it is possible to observe an ideal oscillator output in the frequency domain versus a real oscillator output. In the real situation, the signal spectrum shows symmetrical tails decreasing as $1/\omega_m^2$, where ω_m is the (angular) frequency offset from ω_0, which are referred to as the oscillator phase noise. This $1/\omega_m^2$ dependence, suggests that a sort of white noise is appearing in the circuit which affects the signal integrity [96]. Fig. 2.11b, illustrates what happens when a VCO is used in a receiver for down-conversion, first in an ideal case where the LO signal does not have phase noise, and then, in a real case where the LO signal has phase noise. It can be seen in the latter, that the down-converted signals have overlapping spectra with the wanted signal, after the down-conversion operation, suffering from significant noise contribution due to the tail of the interferer.

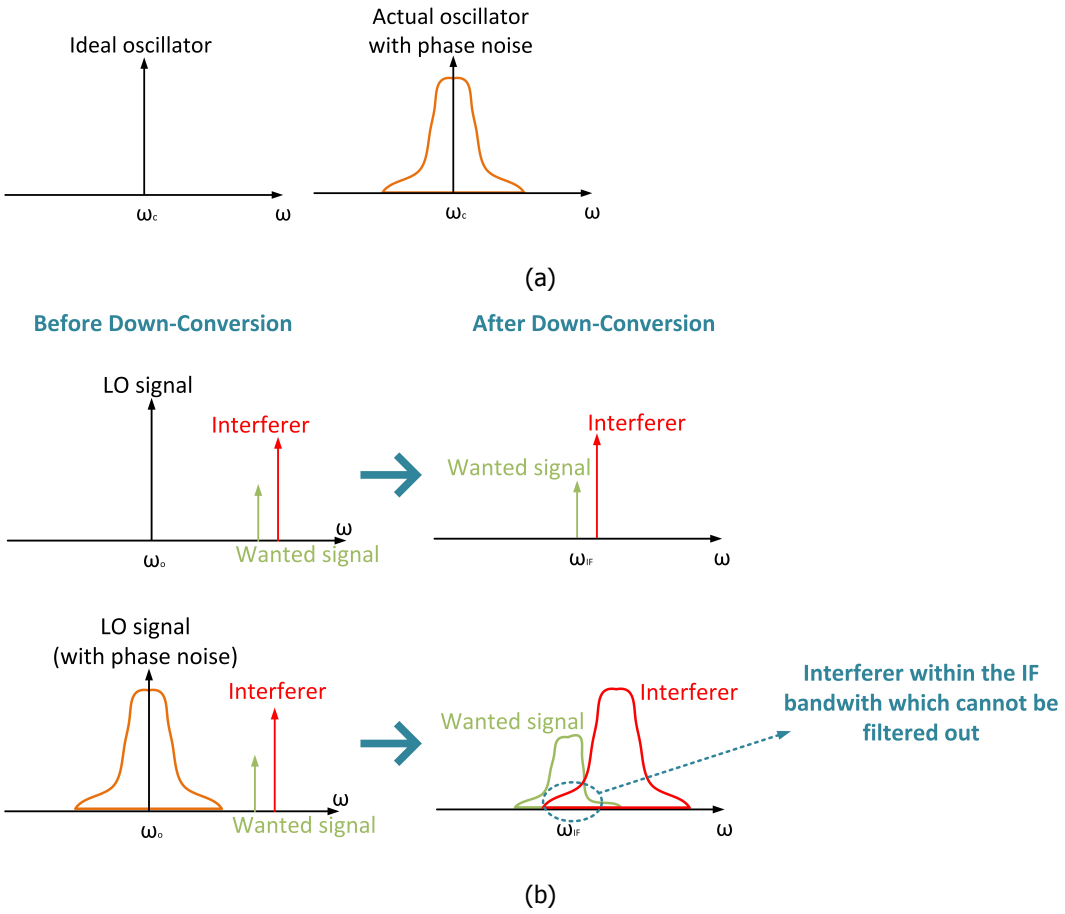


Figure 2.11: (a) Illustrating the meaning of phase noise and (b) Phase noise problem in down-conversion receivers.

Output Swing

The output swing is the value of the amplitude of the signal generated by the oscillator. It can be measured in Volts, which is then called voltage output swing, V_{OUT}, or in dBm, which is called power output swing, P_{OUT}. This value is especially important when the oscillator polarizes a mixer (e.g., receiver). Usually, the VCO will polarize the gate of a MOS transistor of the mixer. Therefore, this value should be as high as possible because it will make the switching operation of the MOS transistors of the mixer faster and, therefore, it will decrease the noise introduced in the circuit.

2.2.3. Mixer

The mixer is a circuit which receives two different input signals (the RF and LO signals) at two different frequencies and outputs a signal at a different frequency (the so-called IF signal). This output frequency is the difference between the input frequencies, therefore, the designer can translate any input frequency to any IF frequency by tuning the LO signal. The mixer symbol is shown in Fig. 2.12.

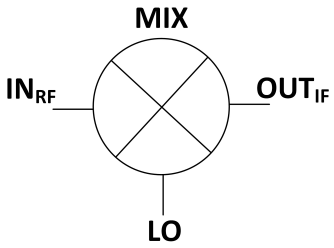


Figure 2.12: Mixer symbol.

The most important performance parameters for the mixer are the following.

Conversion gain

As for the LNAs, the gain quantifies the ability of the mixer to increase the amplitude of the input signal. However, for the mixers the gain is referred to as conversion gain CG because the input and output signal are not at the same frequency.

Linearity

The linearity is also an important metric for the mixer. Since it was already introduced for the LNA, no additional discussion is required here.

Port-to-Port isolation

Similarly to the LNA, the mixer port-to-port isolation is a measure of how well the mixer ports are separated from each other in terms of unwanted signal coupling. This is very important because the LO-RF feedthrough results in LO leakage to the LNA, whereas RF-LO feedthrough allows strong interferer in the RF path to interact with the LO and driving the mixer. The LO-IF feedthrough is also

very important because if a relatively high feedthrough exists from the LO port to the IF the following stage could be desensitized. Desensitization is a phenomena that may happen in receivers, where a strong interferer is present at the output of the receiver and, therefore, the receiver cannot identify the wanted signal [92]. The required isolation levels depend on the environment, but typically, an isolation of 30dB is in most cases considered 'high isolation' [92].

Noise Figure

The mixer noise figure analysis deserves special attention. As previously mentioned, all mixers fold the RF spectrum around the LO frequency, creating an output that contains the summation of the spectrum on both sides. In low-IF architectures, one of these contributions is typically considered spurious and the other intended. Therefore, image reject filtering is used to largely remove one of these responses. On the other hand, in zero-IF receivers, the case is different, because both sidebands are converted and used for the wanted signal. Due to this fact, different noise definitions arise: the single-sideband (SSB) noise and the double-sideband (DSB) noise figure.

The single-sideband noise figure (NF_{SSB}), assumes that the noise from both sidebands is folded into the output signal. However, since only one of the sidebands is useful for conveying the wanted signal, the other is filtered. Therefore, the noise level is doubled, without doubling the signal level, which naturally results in a 3dB increase in noise figure (see Fig. 2.13).

The single-sideband (SSB) noise figure, which characterizes a low-IF receiver, is given by,

$$NF_{SSB} = 10log_{10}(\frac{S_{RF}/N_{RF+IM}}{(S/N)_{IF}}) \tag{2.11}$$

where

- S_{RF} is the signal power at the RF frequency
- N_{RF+IM} is the noise power contributions from the RF and the image (IM) frequency
- $(S/N)_{IF}$ is the signal-to-noise ratio at the intermediate frequency (IF).

On the other hand, the double-sideband noise figure (NF_{DSB}) assumes that both responses of the mixer contain parts of the wanted signal and, therefore, the noise is folded alongside with the corresponding signal. Therefore, the total NF is not impacted (see Fig. 2.14), because the signal is also translated. The double-sideband (DSB) noise figure characterizes a zero-IF receiver, and is given by,

$$NF_{DSB} = 10log_{10}(\frac{S_{RF+IM}/N_{RF+IM}}{(S/N)_{IF}}) \tag{2.12}$$

where

- S_{RF+IM} is the signal power contribution at the RF and the IM frequency.

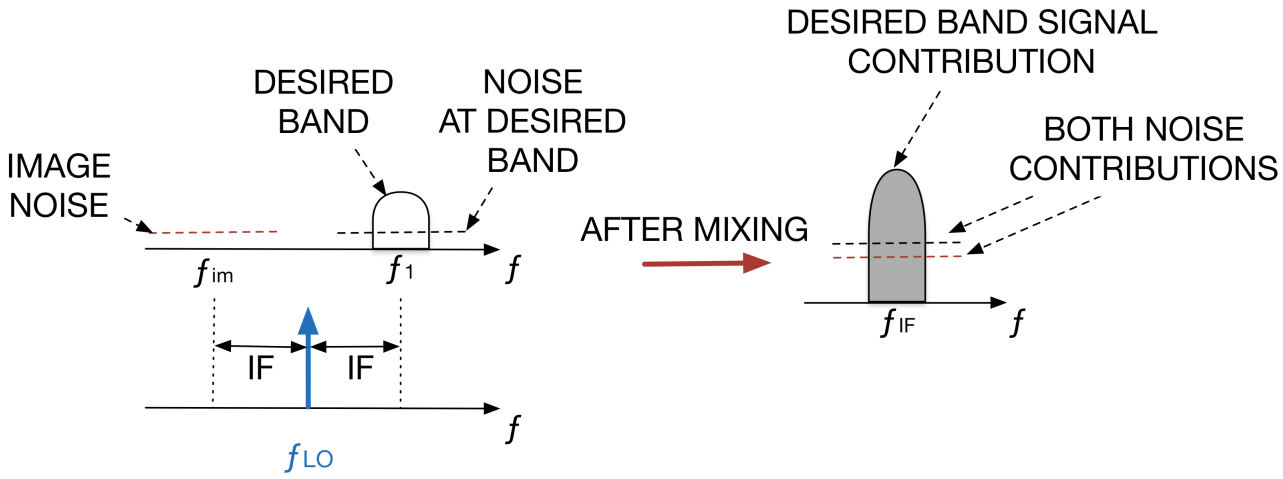


Figure 2.13: Illustrating the NF_{SSB} in mixers.

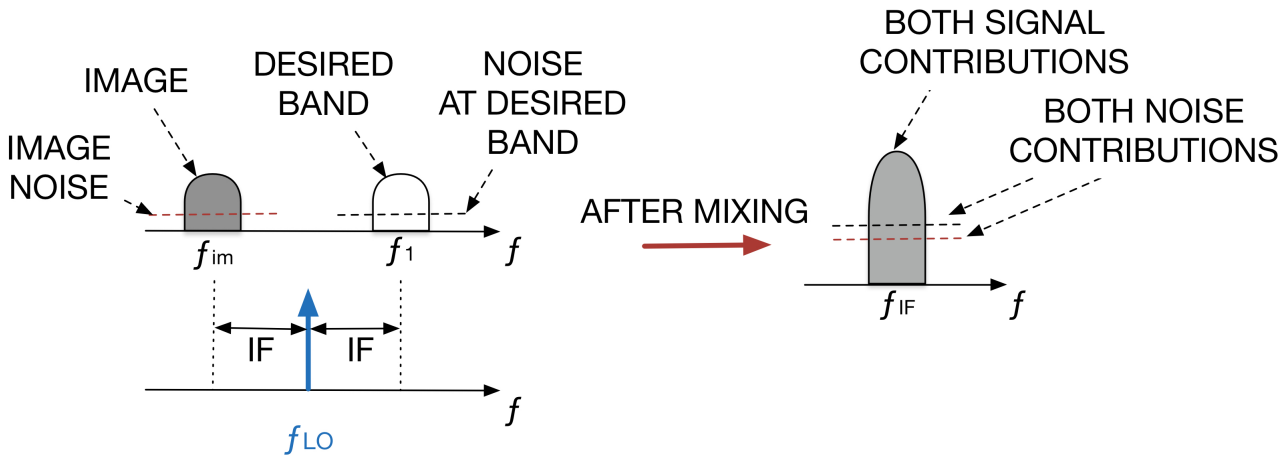


Figure 2.14: Illustrating the NF_{DSB} in mixers.

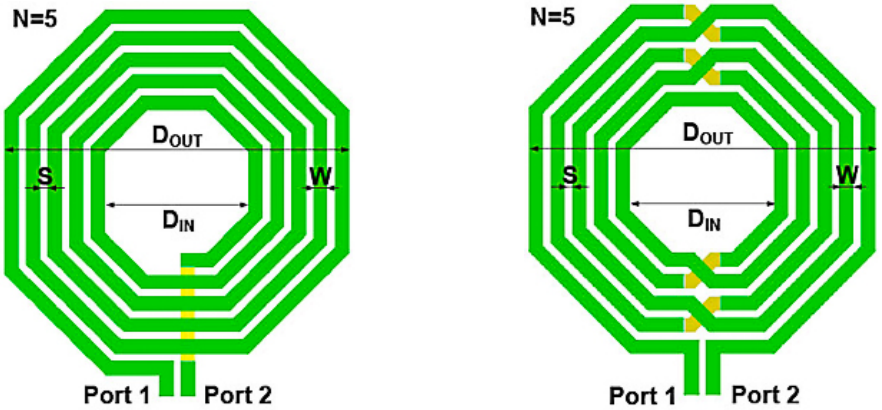
3

Modeling and Synthesis of Radio-Frequency Integrated Inductors

This Chapter discusses the modeling and synthesis of integrated inductors. In Section 3.1, typical inductor topologies are shown, as well as its geometric and performance parameters. Furthermore, the inductor typical behavior over frequency is illustrated in order to give some design insights for this passive component. It is important to know the geometric and performance parameters of this device in order to understand how can the device be modeled and designed. Afterwards, in Section 3.2, two different inductor models are presented: a physical model, which relates analytical equations to a set of electrical components, which are able to emulate the behavior of the inductor, and, a surrogate model, based on machine learning techniques, which is able to capture the behavior of the inductor by learning from a set of $training$ samples, and, afterwards, estimate its performances. Furthermore, in the same Section, an accuracy comparison is performed between such physical and surrogate models. In Section 3.3 different optimization algorithms, both single- and multi-objective are used in order to synthesize integrated inductors. Some comparisons will be performed in order to find out which are the best optimization strategies to synthesize inductors in terms of accuracy and efficiency. Finally, Section 3.4 presentes a tool that was developed incorporating the surrogate models presented in 3.2 and that has the ability to design and optimize several inductor topologies using single- and multi-objective optimization algorithms. Furthermore, the tool also allows the user to build new inductor models, for new inductor topologies and technologies.

3.1. Integrated Inductor Design Insights

Inductors in RF integrated circuits are typically built by using two metal layers, with an intermediate dielectric layer. In Fig. 3.1, the shapes of an octagonal asymmetric and symmetric spiral inductors are illustrated. The geometry of these inductors is usually defined by four geometric parameters: number of turns (N), inner diameter (D_{in}) (or alternatively the outer diameter (D_{out})), turn width (w) and spacing between turns (s).



(a) Octagonal asymmetric inductor topology.

(b) Octagonal symmetric inductor topology.

Figure 3.1: Different inductor topologies.

The most relevant inductor performances are the equivalent inductance, L_{eq}, and the quality factor, Q_{eq}. These performance parameters can can be easily obtained from the S-Parameters of the two-port structure representation of the inductor. For the asymmetric topology, the inductor is measured in single ended mode (SEM), and, therefore, the following formulas can be used in order to calculate L_{eq}, and Q_{eq} [97],

$$\begin{aligned} S_{SEM} &= S_{11} - \frac{S_{12} \cdot S_{21}}{1 + S_{22}} \\ Z_{eq} &= Z_0 \cdot \frac{1 + S_{SEM}}{1 - S_{SEM}} \end{aligned} \tag{3.1}$$

where Z_{eq} is the equivalent input impedance and Z_0 the characteristic impedance of the device (usually 50Ω). For the symmetric topology, the inductor is measured in differential mode (DM) and, the following formulas can be used [97],

$$\begin{aligned} S_{DM} &= \frac{S_{11} - S_{12} - S_{21} + S_{22}}{2} \\ Z_{eq} &= 2 \cdot Z_0 \cdot \frac{1 + S_{DM}}{1 - S_{DM}} \end{aligned} \tag{3.2}$$

After obtaining the equivalent input impedance, Z_{eq}, (either for the asymmetric or symmetric inductor), L_{eq}, and the quality factor, Q_{eq}, are calculated as follows,

$$L_{eq}(f) = \frac{Im[Z_{eq}(f)]}{2\pi f} \tag{3.3}$$

$$Q_{eq}(f) = \frac{Im[Z_{eq}(f)]}{Re[Z_{eq}(f)]} \tag{3.4}$$

where f stands for frequency. In Fig. 3.2, three different plots of the inductance and quality factor as a function of the frequency are illustrated. An important parameter is the self-resonance frequency, SRF, which is defined as the frequency at which the imaginary part of Z_{eq} is zero, or, equivalently, the frequency at which the behavior of the inductor changes from inductive to capacitive (see Eq. (3.3)). While designing and inductor, the designer is usually interested in obtaining the inductance at the operation frequency and its quality factor. It is also important to notice that inductors represent a large percentage of the RF circuit area, and therefore, they should be designed with the smallest area occupation since fabrication cost grows linearly with area. The area can be immediately calculated from the geometric parameters and does not need a model for its estimation.

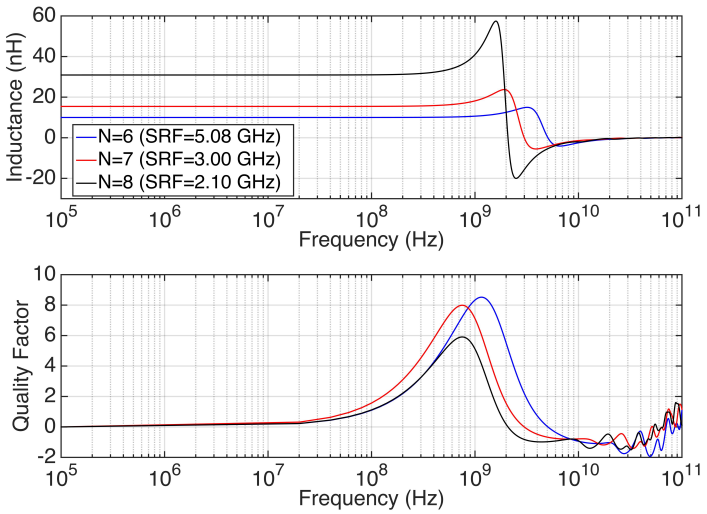


Figure 3.2: Illustrating inductance and quality factor as a function of frequency for three different inductors

After presenting the geometric and performance parameters of integrated inductors, in the following Section, two different techniques will be studied in order to model these passive components and estimate their performance parameters. The basic idea of the modeling techniques is to estimate the inductors performances from its geometric parameters. Both models will be compared in terms of accuracy and efficiency.

3.2. Modeling Methodologies: Physical vs. Surrogate models

In this section, two different modeling techniques for integrated inductors are presented. Both techniques have their advantages and disadvantages, and provide different trade-offs to RF designers. These trade-offs will be analyzed in the following section. For the model error assessment, a statistical study of an octagonal asymmetric spiral inductor topology in a 0.35μm-CMOS technology is performed using both models and the results are compared.

3.2.1. Physical Modeling of Integrated Inductors

An inductor physical model relates a set of equations to a set of electrical components. Afterwards, this model can be used in an electrical simulator in order to emulate the inductor behavior. Also, the Z_{eq} can be analytically calculated in order to get the inductor performances using Eq. (3.3) and Eq. (3.4). One of the most well-known and widespread used physical models, is the π-model, illustrated in Fig. 3.3 and presented in [50].

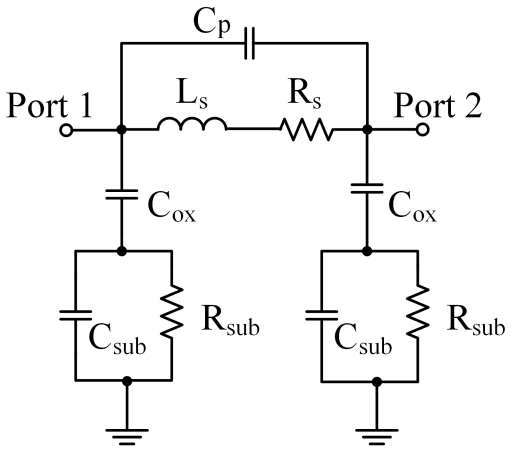


Figure 3.3: Typical integrated inductor physical model (π-model)

The lumped-element circuit, shown in Fig. 3.3, tries to model the inductor through the branch consisting of L_s, R_s and C_p. The series resistance, R_s, arises from metal resistivity of the spiral inductor and is closely related to the quality factor, being a key issue for inductor modeling. The series feedforward capacitance, C_p, is considered as the overlap capacitance between the spirals and the underpass metal lines, also called C_l. In order to increase the accuracy of the model, not only the metal spiral but also the $surrounding$ environment has to be taken into account. Therefore, both the oxide layer and the silicon substrate have to be modeled. In order to model the oxide layer, a capacitance C_{ox} is set between the spiral and the substrate. Afterwards, in order to model the silicon substrate, a capacitance C_{sub} and a resistance R_{sub} are used. Fig. 3.4 illustrates these lumped elements and its relation to the inductor physical implementation.

Physical π-Model

As previously mentioned, each lumped element of the π-model can be calculated through an analytical equation. These will be presented in this sub-Section.

The resistance R_s, which emulates the series resistance of the inductor, is given by,

$$R_s = \frac{\rho \cdot l}{w \cdot \delta \cdot (1 - e^{-t/\delta})} \tag{3.5}$$

where l is the conductor length, ρ is the resistivity of the material, w is the metal width and t the metal

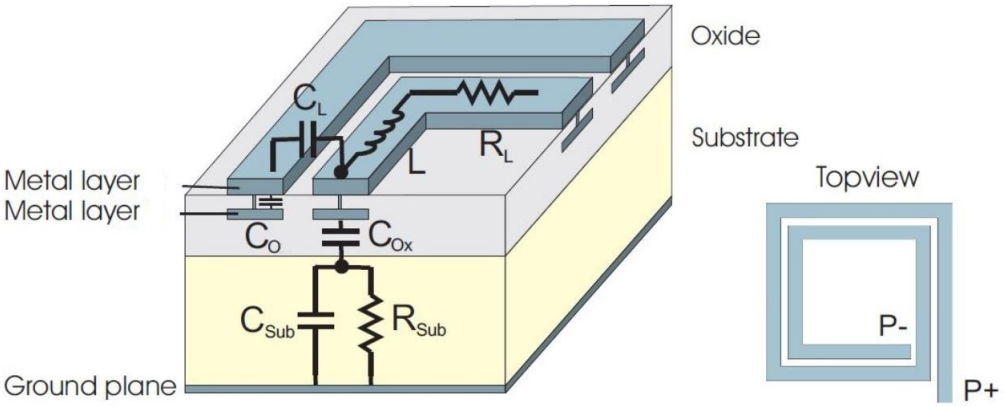


Figure 3.4: Physical definition of the lumped-elements of the inductor model.

thickness. The skin depth, δ, is given by the following equation [98],

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \tag{3.6}$$

where f is the frequency and μ is the permeability of the metal. The oxide capacitance C_{ox} can be approximated by,

$$C_{ox} = \frac{1}{2} \cdot l \cdot w \cdot \frac{\varepsilon_{ox}}{t_{ox}} \tag{3.7}$$

where ε_{ox} is the relative permittivity of the oxide and t_{ox} the oxide thickness.

The silicon substrate is modeled with the resistance R_{sub} and the capacitance C_{sub}. The resistance is used in order to model the resistivity of the substrate, and is given by,

$$R_{sub} = \frac{2}{l \cdot w \cdot G_{Sub}} \tag{3.8}$$

where G_{sub} is the conductance per unit area for the silicon substrate and can be approximated by,

$$G_{sub} = \frac{\sigma_{S_i}}{h_{S_i}} \tag{3.9}$$

where σ_{S_i} is the conductivity of the silicon substrate and h_{Si} is the thickness of the substrate. Moreover, the substrate capacitance C_{sub} is given by,

$$C_{sub} = \frac{1}{2} \cdot l \cdot w \cdot C_{ms} \tag{3.10}$$

where C_{ms} is the unit length capacitance between the metal and the substrate. Finally, the capacitance C_p is calculated through,

$$C_p = n_{cross} \cdot w^2 \cdot \frac{\varepsilon_{ox}}{t_{M1-M2}} \tag{3.11}$$

where t_{M1-M2} is the oxide thickness between the spiral and the underpass metal layer and n_{cross} is the number of crossovers between the spirals and the underpass metal.

The inductance L_s, shown in Fig. 3.3, represents the series inductance and can be calculated through several formulas and techniques [99]. However, one of the most used is the Greenhouse

formula [100], given by the following equation,

$$L = 2l\left\{ln\left[\frac{2l}{w+t}\right] + 0.50049 + \frac{w+t}{3l}\right\}(nH) \tag{3.12}$$

where L is the series inductance. By using Eqs. (3.5)-(3.12), the designer is able to relate the inductor geometric parameters to the values of the electrical components of the lumped-element circuit given in Fig. 3.3, and, therefore, model, design and simulate a given integrated inductor with any set of geometric parameters.

Physical Segmented Model

However, with the continuing shrinking size of CMOS and with higher operating frequencies, the analytical equations previously presented and the π-model itself, is usually too simple to capture all the inductor physics and, therefore, more accurate models have been proposed. The physical model used in this thesis is based on the segmented model approach [101], where the inductor is divided into segments and each segment is characterized with an individual π-model equivalent circuit, as shown in Fig. 3.5.

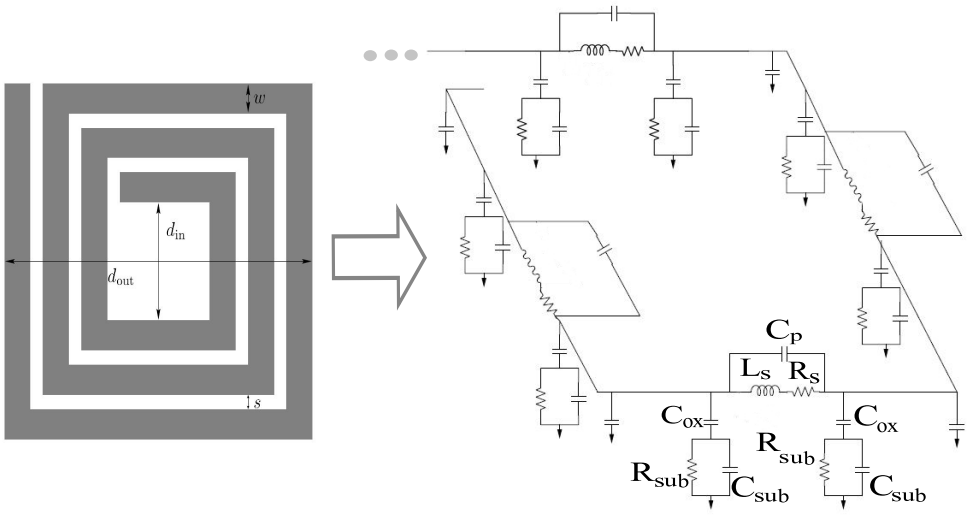


Figure 3.5: Square inductor, its physical parameters and the π-model equivalent circuit for each turn of the inductor

In this segmented model, the capacitances are calculated by using a more complex method, which is the distributed capacitance model (DCM) [102]. This method provides more accurate results than the analytical equations used in the simple π-model. This DCM method includes high frequency effects, such as the skin and proximity effects, which, therefore, make the model suitable to be used up to higher frequencies. To calculate the capacitances, we first define the lengths of each inductor segment as l_1, l_2,..., l_n, and the total length as l_{tot}=l_1+l_2+...+l_n, where l_n is the length of the last segment of the outer turn. Afterwards, we define,

$$h_k = \sum_{k=1}^{n} \frac{l_k}{l_{tot}} \tag{3.13}$$

and the capacitances can be calculated with the following formulas [102]:

$$C_p = \sum_{k=1}^{n} x \cdot \frac{4}{3} C_{mm} l_k \cdot \frac{\left[(h_k - h_{k-1})^2 + (h_{k+1} - h_k)^2 + (h_{k+1} - h_k)(h_k - h_{k-1})\right]}{(h_{k+1} - h_{k-1})^2} \tag{3.14}$$

$$C_{ox} = \sum_{k=1}^{n} x \cdot \frac{1}{2} \cdot \frac{4}{3} C_{ms} l_k \cdot \frac{\left[(1 - h_{k-1})^2 + (1 - h_k)^2 + (1 - h_k)(1 - h_{k-1})\right]}{3(2 - h_k - h_{k-1})^2} \tag{3.15}$$

An empirical scale factor x, which is the same for both equations, can be used as a fitting parameter in order to adjust the capacitance values to the adopted technology. The 1/2 factor in C_{ox} is due to the fact that the capacitance is divided into two in the π-model. C_{mm} and C_{ms} are the unit length capacitance between the metal spirals and the unit length capacitance between the metal and the substrate, respectively. Normally, these are extracted from measured data, but they can be approximated as follows [103],

$$C_{mm} = \frac{\varepsilon_0 \varepsilon_{SiO_2} \cdot t}{s} \tag{3.16}$$

$$C_{ms} = \frac{\varepsilon_0 \varepsilon_{SiO_2} \cdot w}{h_{SiO_2}} \tag{3.17}$$

where ε_0 is the vacuum permittivity and $\varepsilon_{s_iO_2}$ is the relative permittivity of silicon dioxide. $h_{s_iO_2}$ is the distance from the metal to substrate (the silicon dioxide thickness).

The substrate resistance is crucial for accurately modeling of the peak Q and the shape of the Q curve, along with the series resistance R_s. This resistance can be calculated, according to [104], by,

$$R_{sub} = \frac{2}{l \cdot w \cdot G_{sub}} \tag{3.18}$$

where l is the segment length and G_{sub} is the conductance per unit area for the silicon substrate and can be approximated, according to [103], by,

$$G_{sub} = \frac{\sigma_{Si}}{h_{Si}} \tag{3.19}$$

where σ_{Si} is the conductivity of the silicon substrate and h_{Si} is the thickness of the substrate.

The substrate capacitance can normally be approximated using a simple fringing capacitance model as the one given in [104]. However, to extend our model to high frequencies with more accuracy, we use the DCM model technique to calculate the substrate capacitance C_{sub},

$$C_{sub} = \sum_{k=1}^{n} x \cdot \frac{1}{2} \cdot \frac{4}{3} C_{ss} l_k \cdot \frac{\left[(1 - h_{k-1})^2 + (1 - h_k)^2 + (1 - h_k)(1 - h_{k-1})\right]}{3(2 - h_k - h_{k-1})^2} \tag{3.20}$$

Again, x is the same fitting factor used for previous equations, the 1/2 factor in C_{sub} is due to the fact that the capacitance is divided into two in the π-model and C_{ss} is the length capacitance between the substrate and the ground plane, which can be approximated by the following equation [103]:

$$C_{ss} = \frac{\varepsilon_0 \varepsilon_{s_i} \cdot w}{h_{S_i}} \tag{3.21}$$

By using the previous formulas to calculate the values of R_s, C_p, C_{ox}, C_{sub} and R_{sub} (given in Eq. (3.14)-(3.20)) a more reliable inductor model can be developed. Furthermore, the Greenhouse formula, presented in Eq. (3.12), used for L_s, only takes into account the series inductance and not the mutual inductances that appear in integrated inductors, degrading therefore the accuracy of the inductance calculation. Therefore, in order to provide a more accurate inductance calculation, the physical model developed in this thesis uses a set of formulas which describe the individual and mutual inductances of any piecewise structure, therefore being able to calculate the series inductance for any inductor topology.

In 1929, Grover derived formulas for inductance calculation between filaments in several different positions [105]. Greenhouse later applied these formulas to calculate the inductance of a square shaped inductor by dividing the inductor into straight-line segments, as illustrated in Fig. 3.5, and evaluating the inductance by adding up the self inductance of the individual segments and mutual inductance between segments [100]. Some authors call this method the ”mutual inductance approach” [106].

Here, the evaluation of the series inductance, L_s, for an octagonal inductor will be given as an example in order to illustrate this mutual inductance approach. Further generalization of the formula for an n-side inductor is also addressed. For hexagonal layouts, the angle between segments is 120 degrees, and for octagonal layouts the angle is 135 degrees and so on. The total inductance of an inductor is given by,

$$L_s = L_0 + M_{p+} - M_{p-} - M_{lm} \tag{3.22}$$

where L_s is the total series inductance of the inductor, L_0 is the self inductance of each segment, M_{p+} is the mutual inductances of parallel segments, where the current flows in the same direction whereas M_{p-} accounts for mutual inductance of the parallel segments where currents flow in the opposite directions [100]. Furthermore, M_{lm} accounts for all the different types of mutual inductances resulting from non-parallel segments. These mutual inductances should be summed or subtracted depending on the flow of the current.

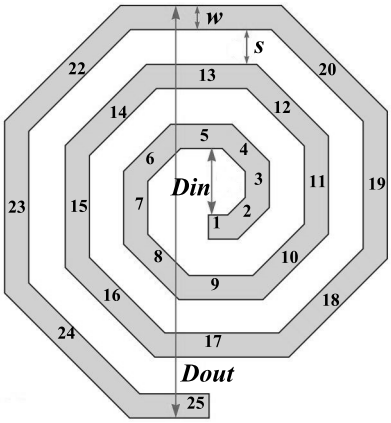


Figure 3.6: Twenty-five segment octagonal spiral inductor layout.

For the particular case of the inductor in Fig. 3.6 it is possible to calculate the L_s value through,

$$L_s = L_1 + L_2 + \ldots + L_{25}$$

(Self inductance)

$$+ 2(M_{1,9} + M_{2,10} + M_{3,11} + M_{4,12} + M_{5,13} + M_{6,14} + \ldots + M_{17,25})$$

(Positive mutual inductances)

$$- 2(M_{1,5} + M_{2,6} + M_{3,7} + M_{4,8} + M_{5,9} + M_{10,6} + \ldots + M_{25,21})$$

(Negative mutual inductances)

$$- 2(M_{1,2} + M_{2,3} + M_{24,25} + \ldots + M_{1,3} + M_{3,5} + M_{23,25} +$$
$$\ldots + M_{1,11} + M_{2,12} + \ldots + M_{16,25})$$

(Mutual inductances as shown in Fig. 3.7 - 3.11) (3.23)

Due to the magnitude and phase of the currents, the mutual inductances are assumed identical in all sections, hence $M_{a,b}$=$M_{b,a}$. In order to calculate the self-inductance, L_0, the Greenhouse formula given in Eq. (3.12), may be applied. For the evaluation of the mutual inductances, the formulas deducted by Groover [105] are applied. For the case of two parallel segments, as depicted in Fig. 3.7 (e.g., $M_{1,9}$ in Fig. 3.6), where d is the distance between the parallel with lengths l and m, and r and q represent the difference between the length of the segments. The mutual inductances can be calculated by,

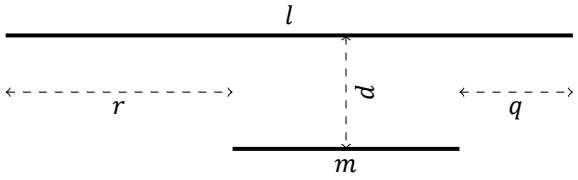


Figure 3.7: Parallel segments.

$$2M = (M_{m+r} + M_{m+q}) - (M_r + M_q) \tag{3.24}$$

Each $M_{i,j}$ is calculated with the following formula,

$$M = 2 \cdot l \cdot U \tag{3.25}$$

where U, is calculated by,

$$U = ln\left[\frac{l}{d} + \sqrt{1 + \left(\frac{l}{d}\right)^2}\right] - \sqrt{1 + \left(\frac{d}{l}\right)^2} + \frac{d}{l} \tag{3.26}$$

where d is the distance between segments, which is considered as the geometric mean distance (GMD) between segments and calculated by,

$$ln(GMD) = ln(p) - \frac{w^2}{12p^2} - \frac{w^4}{60p^4} - \frac{w^6}{168p^6} - \frac{w^8}{360p^8} - \frac{w^{10}}{660p^{10}} - \cdots \tag{3.27}$$

where, p is the pitch of the two wires and w is the width of the segments in study. Note that, for the particular case of a square inductor, the series inductance calculation will not comprise the mutual inductance between two consecutive segments, since their mutual inductance is zero (because the angle between them is 90 degrees). However, for the specific case of the octagonal inductor under study, the angle between them is not 90 degrees, and therefore, the mutual inductance must be taken into account. An example for mutual inductance for segments which are connected at one end, such as $M_{4,3}$, is present in Fig. 3.8.

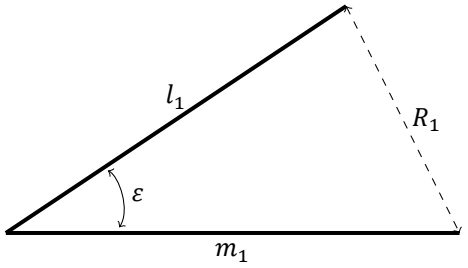


Figure 3.8: Segments which are connected at one end.

This type of mutual inductance is calculated through [105]:

$$M_{lm} = 2cos\varepsilon\left[l_1 tanh^{-1}\left(\frac{m_1}{l_1+R_1}\right)+m_1 tanh^{-1}\left(\frac{l_1}{m_1+R_1}\right)\right] \tag{3.28}$$

In Eq. (3.28), l_1 and m_1 are the lengths of the segments and R_1 is the distance between the segment ends, and can be calculated by,

$$R_1^2 = 2l^2(l - cos\varepsilon) \tag{3.29}$$

It is also possible to use one of the following relations to substitute either R_1 or ε.

$$\cos\varepsilon = \frac{l^2+m^2-R_1^2}{2lm} \tag{3.30}$$

$$\frac{R_1^2}{l^2} = 1+\frac{m^2}{l^2}-2\frac{m}{l}\cos\varepsilon \tag{3.31}$$

The case of mutual inductance where the intersection point is lying outside the two filaments, for example, $M_{3,5}$, is given in Fig. 3.9, whereas the case where the intersection point lies upon one filament, which is the most complex case, such as $M_{5,14}$, is presented in Fig. 3.10.

The mutual inductances in Fig. 3.9 and Fig. 3.10 are calculated by the following equation,

$$M_{lm} = 2\cos\varphi\left[(M_{\mu+l,\nu+m}+M_{\mu\nu})-(M_{\mu+l,\nu}-M_{\nu+m,\mu})\right] \tag{3.32}$$

The general case for mutual inductances between segments is given in Fig. 3.11, which can be calculated with the following equation.

$$M_{lm} = 2cos\varepsilon\cdot\left[(\mu+l)\cdot tanh^{-1}\left(\frac{m}{R_1+R_2}\right)+(\nu+m)\cdot tanh^{-1}\left(\frac{l}{R_1+R_4}\right)\right.$$
$$\left.-\mu\cdot tanh^{-1}\left(\frac{m}{R_3+R_4}\right)-\nu\cdot tanh^{-1}\left(\frac{l}{R_2+R_3}\right)\right] \tag{3.33}$$

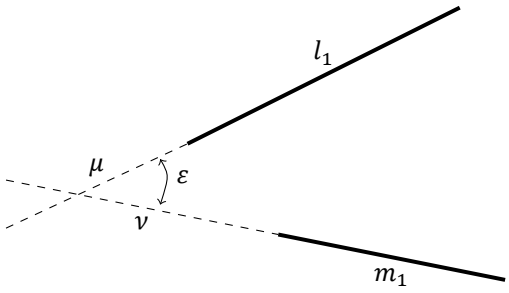


Figure 3.9: Case for when the intersection point is lying outside the two filaments.

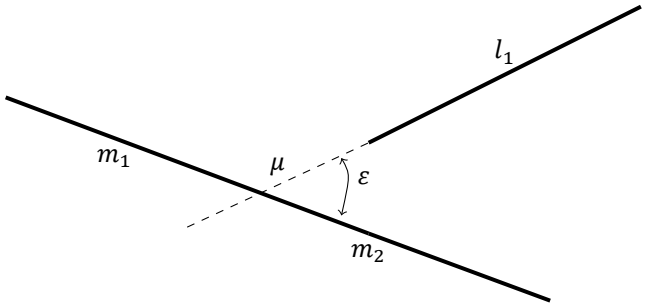


Figure 3.10: Case for when the intersection point lies upon one filament.

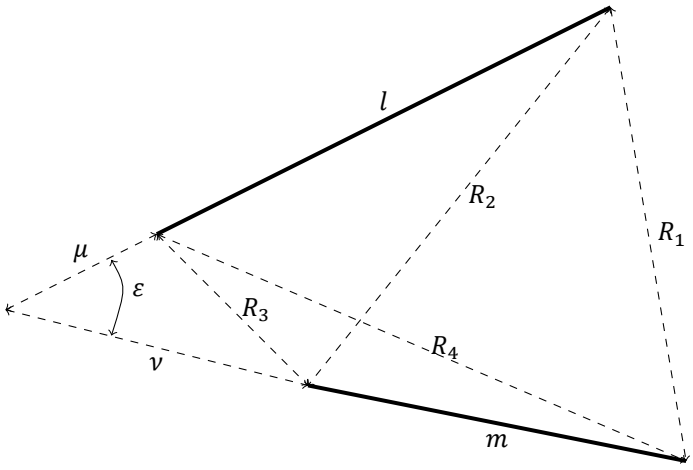


Figure 3.11: General case for two segments placed in the same plane.

While the so-called intermediary geometric parameters R_1 to R_4 can be calculated with the following set of formulas,

$$R_1^2 = (\mu + l)^2 + (\nu + m)^2 - 2(\mu + l)(\nu + m)\cos\varepsilon \tag{3.34}$$

$$R_2^2 = (\mu + l)^2 + \nu^2 - 2\nu(\mu + l)\cos\varepsilon \tag{3.35}$$

$$R_3^2 = (\mu)^2 + \nu^2 - 2\nu\mu\cos\varepsilon \tag{3.36}$$

$$R_4^2 = (\mu)^2 + (m + \nu)^2 - 2\mu(\nu + m)\cos\varepsilon \tag{3.37}$$

The following needed parameters in order to calculate M_{lm} in Eq. (3.33), are given by,

$$2\cos\varepsilon = \frac{\alpha^2}{lm} \tag{3.38}$$

$$\alpha^2 = R_4^2 - R_3^2 + R_2^2 - R_1^2 \tag{3.39}$$

$$\mu = \frac{l\left[2m^2(R_2^2 - R_3^2 - l^2) + \alpha^2(R_4^2 - R_3^2 - m^2)\right]}{4l^2m^2 - \alpha^2} \tag{3.40}$$

$$\nu = \frac{m\left[2l^2(R_4^2 - R_3^2 - m^2) + \alpha^2(R_2^2 - R_3^2 - l^2)\right]}{4l^2m^2 - \alpha^2} \tag{3.41}$$

Using Eq. (3.33) and the set of equations presented in (3.34)-(3.41), the inductance of any piecewise structure can be approximated. However it is easy to understand that when one increases the number of segments, the difficulty of calculation increases exponentially due to the number of new mutual inductances that appear [107].

Physical Segmented Model Accuracy Assessment

In order to evaluate the accuracy of this physical model, 240 test inductors were generated covering the design space specified in Table 3.1. The samples were generated following a Latin hypercube sampling (LHS) distribution [108]. These 240 inductors were EM simulated with ADS *Momentum* [109], in order to have a benchmark comparison for accuracy. The technology selected was a 0.35μm CMOS technology, for which the process information required for EM simulation was available. It should be said, that the space between turns, s, was maintained as the minimum size permitted by the technology, because increasing this value does not bring advantages in the inductor performances [55].

The 240 generated inductors were separated by number of turns (30 per turn). The inductors were simulated at two different frequencies with the physical model presented in the previous Sections and

Table 3.1: Inductor variable ranges for the LHS sampling.

Parameter	Minimum	Grid	Maximum
N	1	1	8
D_{in} (μm)	10	1	300
w (μm)	5	0.05	25
s (μm)	2.5	-	2.5

the performances obtained were compared with the values obtained through EM simulation. An error assessment was performed using the following equation,

$$Error = \frac{EM_{sim} - Model}{EM_{sim}} \times 100 \quad (\text{in } \%) \tag{3.42}$$

It is possible to observe in Table 3.2 that the model errors are very high both for inductance (ΔL) and quality factor (ΔQ), and that the error increases for inductor with higher number of turns. This fact can be explained, by two different facts: on the one hand inductors with higher number of turns have more segments, increasing the calculation complexity and, therefore, introducing more errors. On the other hand, inductors with higher number of turns are more difficult to model because its behavior is more abrupt. Therefore it is possible to conclude that this physical model is not sufficiently accurate for modeling integrated inductors.

Table 3.2: Average error (in %) of inductance and quality factor for 240 test inductors.

N	20 MHz		2.5 GHz	
	ΔL (%)	ΔQ (%)	ΔL (%)	ΔQ (%)
1	18.35	61.20	21.55	31.54
2	10.82	43.96	20.44	34.26
3	13.96	40.53	51.09	46.36
4	13.31	35.41	66.40	69.79
5	10.23	25.07	98.64	127.55
6	10.15	24.36	107.93	141.40
7	12.61	27.95	150.34	229.04
8	12.80	28.72	190.42	511.66

The performances of integrated inductors are highly affected by phenomena such as Eddy currents and proximity effects. Even thought the segmented model, uses the DCM capacitance model, which already takes into account the Eddy currents and proximity effects, the prediction of these effects is not entirely accurate. Therefore, in some areas of the design space where these effects are dominant, e.g., smaller D_{in} and large w, the error of the model is large. Since the model does not accurately estimate the inductor performances in these areas and in order to increase the accuracy, the design space was reduced to inductors with D_{in}>70μm and w<15μm.

Apart from the design space reduction, several fitting factors (over the analytical equations) were tested in order to reduce the model error. By executing some statistical studies in order to fine tune

the physical model, it was found that by setting the fitting factor, x, of $\frac{1}{2}$ to the C_p, C_{ox} and C_{sub} capacitances (in Eq. (3.14), (3.15) and (3.20)), the model errors can be decreased, as it can be seen in Table 3.3.

Table 3.3: Average error (in %) of inductance and quality factor for 106 test inductors: reduced design space and using fitting factors

N	20 MHz		2.5 GHz	
	ΔL (%)	ΔQ (%)	ΔL (%)	ΔQ (%)
1	3.70	19.62	3.98	5.28
2	1.77	11.75	0.89	3.83
3	1.95	13.26	3.68	9.89
4	2.27	13.28	9.44	11.26
5	2.19	7.62	18.27	15.17
6	2.77	8.77	48.76	87.15
7	3.26	9.64	229.83	354.76
8	3.59	10.49	90.87	146.64

For higher number of turns, the model errors increase at high frequencies (2.5GHz), which may be due to the fact that inductors with higher number of turns have its SRF around or lower than 2.5GHz, which means that the inductance and quality factor of inductors is changing very sharply with frequency (see Fig. 3.2). This sharp behavior increases the difficulty of the modeling process, increasing, therefore, the relative error of the model. From the errors shown in Table 3.3, it can be concluded that typical physical models are not suitable for an accurate modeling of integrated inductors, therefore, new techniques must be developed in order to accurately model these components.

3.2.2. Surrogate Modeling of Integrated Inductors

Surrogate modeling is an engineering method used when an outcome of interest of a complex system cannot be easily (or cheaply) measured either by experiments or simulations [108]. An approximate model of the outcome is used instead. This section first describes the basic steps involved in the generation of a surrogate model, and, afterwards, presents the proposed methodology for modeling inductor performances.

Generating a surrogate model usually involves four steps which are briefly described below, indicating the options adopted in this work.

1. Design of experiments:

   The objective of surrogate models is to emulate the output response of a given system. Therefore, the model has to learn how the system responds to a given input. So, the first step in generating surrogate models is to select the input samples from which the model is going to learn. These samples should evenly cover the design space, so that it can be accurately modeled. In order to perform this sampling, different techniques are available, from classical Monte-carlo (MC) to quasi-Monte-carlo (QMC) or LHS [108]. In this Chapter, LHS is used.

2. Accurate expensive evaluation:

   Surrogate models learn from accurate but expensive evaluations. In our work, these accurate evaluations are EM simulations, which are performed with ADS *Momentum* [109]. Depending on the size of the training set, these simulations could even last for weeks. However, these simulations are only performed once for a given fabrication technology, therefore being useful for several years, as technology nodes do not become obsolete in months. Any modeling technique can later be used in order to build a new model using the same training set.

3. Model construction:

   This concerns the core functions used to build a surrogate model. Literature reports approaches based on artificial neural networks (ANN), support vector machines (SVM), parametric macromodels (PM), Gaussian-process or Kriging models, etc [110]. In this thesis, ordinary Kriging models are used. Different Matlab toolboxes like SUMO [111] or DACE [112] support this type of models, being DACE the one finally selected. One of the motivations for using Kriging is that it provides an error estimate. The motivations to select DACE were practical reasons, such as: it is freely available, simple to use and it runs over a widely used software, which is MATLAB [113].

4. Model validation:

   Many different techniques may be used in order to validate the model and assess its accuracy e.g. cross-validation, bootstrapping and subsampling [114]. In this Chapter, in order to validate the model, a set of points was generated independently of the training samples. These samples will be referred to as test samples and were also generated using LHS.

Modeling Strategy

Inductance and quality factor are functions of the frequency. There have been attempts to build frequency-dependent models [115, 116] for integrated inductors. However, surrogate models suffer from exponential complexity growth with the number of parameters. This exponential complexity growth is also valid if the number of training samples increases. In order to alleviate this problem, problem-specific knowledge can be exploited. In this thesis, the modeling of inductors is performed in a frequency-independent fashion. Hence, an independent model is created for each frequency point. This allows to increase the accuracy, highly reduce the complexity of the models and also the time to generate them [60].

The initial strategy to build the model was to create a surrogate model valid in the complete design space. The model was created using 800 inductors generated with the LHS technique. Two different models were developed: one for predicting the inductance and another for the quality factor (denoted as L and Q models, for the sake of simplicity). Please recall that, since the models are frequency-independent, L and Q models have to be created for each frequency point. In order to compare the surrogate and the physical modeling techniques, the technology selected was the same 0.35μm CMOS

technology, and the test samples used were the same used previously. Therefore, these L and Q models were valid for inductors with any given number of turns N, inner diameter D_{in} and turn width w for the ranges shown in Table 3.1. After testing the global surrogate model, against the same 240 inductors previously generated to test the analytical model, it is possible to observe in Table 3.4, that the mean relative error is much lower when compared with the physical model. However, the error is still unacceptably large at higher frequencies.

Table 3.4: Average error (in %) of inductance and quality factor for 240 test inductors: global model for all N

20 MHz		1 GHz		2.5 GHz	
ΔL (%)	ΔQ (%)	ΔL (%)	ΔQ (%)	ΔL (%)	ΔQ (%)
0.03	0.28	0.54	0.62	16.64	3.61

By understanding that the number of inductor turns can only take some discrete values, i.e., in the implementation reported in this thesis, it can only take integer values, it becomes clear that by creating several surrogate models, one for each number of turns (e.g. one model for inductors with two turns, another for inductors with three turns, etc.) the model accuracy can be increased, because the complexity of the modeled design space decreases. The generation of separate surrogate models for each number of turns instead of considering the number of turns as an input parameter of the surrogate model brings several benefits: not only is the accuracy significantly enhanced but also the computational cost is significantly decreased as the computational complexity of the training process grows exponentially with the number of samples. The number of models to create is manageable as the number of turns is typically between 1 and 8. This strategy increases the overall accuracy and efficiency of the model, as shown for the average errors of 240 test inductors in Table 3.5. However, some test inductors still present large L and Q errors, specifically at high frequencies (around 2.5GHz) for inductors with many turns.

Table 3.5: Inductance and quality factor average error for 240 test inductors (in %): one model for each N

N	20 MHz		1 GHz		2.5 GHz	
	ΔL (%)	ΔQ (%)	ΔL (%)	ΔQ (%)	ΔL (%)	ΔQ (%)
1	0.08	0.46	0.09	0.62	0.08	0.54
2	0.06	0.77	0.14	0.89	0.19	0.78
3	0.03	0.37	0.10	0.52	0.15	0.39
4	0.02	0.32	0.16	0.77	0.24	0.92
5	0.01	0.21	0.07	0.36	0.47	0.61
6	0.01	0.17	0.11	0.50	2.39	1.60
7	0.02	0.34	0.11	0.60	21.70	2.20
8	0.01	0.15	0.11	0.44	6.96	2.36

This high error can be explained by the fact that some inductors from the training set have their SRF below or around the 2.5GHz range. Kriging surrogate models assume continuity: if an input variable changes by a small amount, the output varies smoothly. However, in the adopted technology, some

inductors with more than 5 turns, have their SRF close to 2.5GHz, where the inductance does not change smoothly (see Fig. 3.2). Therefore, the use of these inductors during the model construction dramatically decreases the accuracy of the model, because they present a sharp behavior and blur the model creation. Therefore, the accuracy estimation of L and Q of these useful inductors is dramatically increased if only inductors with SRF sufficiently above the desired operating frequency are used for model training. However, this option is only feasible if we can detect which inductors have their SRF sufficiently above the frequency of operation and are, hence, useful.

Therefore, in the proposed strategy, the construction of the model is based on a two-step method:

1. Generate surrogate models for the SRF (for each number of turns) using all training inductors.

2. In order to generate highly accurate surrogate models for L and Q, only those inductors from the training set whose SRF is sufficiently above the operating frequency are used. For example, if the operating frequency is 2.5 GHz, only inductors with SRF>3 GHz are used to generate L and Q models. In Fig. 3.2, it is possible to observe that the selected inductors with eight turns are not useful at 2.5 GHz, since their SRF<3GHz.

Consequently, with this methodology, whenever a test inductor is going to be evaluated, its SRF value is predicted first. If the predicted SRF is below 3 GHz, the inductor is discarded since it is not useful for the selected operating frequency. Otherwise, its inductance and quality factor are calculated using the L/Q models. The algorithm for model training is, therefore, as follows:

TRAINING PHASE

Step 1: Sampling:

Generate set ITS of B inductor training samples for each number of turns using LHS. Generate set IVS of B_x validation samples for each number of turns using LHS.

Step 2: Simulation:

Perform EM simulation of the (B+B_x) samples.

Step 3: SRF modeling:

For each number of turns $i = 1, \ldots, N_{max}$, generate model of self-resonance frequency using set ITS.

Step 4: Inductor selection:

Extract from ITS the set of training inductors ITS^* with $SRF > f_0 + \Delta f$ where f_0 is the frequency of operation and Δf is a safety margin.

Step 5: L/Q modeling:

For each number of turns, $i = 1, \ldots, N_{max}$, generate L/Q model at frequencies of interest using set ITS^*.

Step 6: Validation:

Use set IVS to validate the accuracy of the generated models.

Model training for a given technology and frequency of operation is performed only once. This model can be used as many times as needed according to the following algorithm:

EVALUATION PHASE

For a set IES of C inductors to evaluate $i = 1, ..., C$ do:

Step 1: SRF evaluation

Predict the self-resonance frequency of the $i-th$ inductor using the SRF model.

Step 2:

If the predicted self-resonance frequency $SRF_{pre} > f_0 + \Delta f$ go to Step 3. Otherwise, discard $i-th$ inductor as a non-valid inductor for the desired frequency of operation and go to Step 1.

Step 3: L/Q evaluation

Predict L and Q of $i-th$ inductor at frequencies of interest using the L/Q model.

In order to evaluate the validity of the proposed strategy, the 240 test inductors were evaluated for three different frequencies. The model errors for L and Q are shown in Table 3.6 and for the SRF in Table 3.7. It can be concluded that by following this modeling strategy, the model error for inductance and quality factor is always below 1% for L and Q (even at 2.5GHz).

Table 3.6: Inductance and quality factor average error for 240 test inductors (in %): one model for each N filtered by SRF

N	20 MHz		1 GHz		2.5 GHz	
	ΔL (%)	ΔQ (%)	ΔL (%)	ΔQ (%)	ΔL (%)	ΔQ (%)
1	0.08	0.46	0.08	0.62	0.08	0.54
2	0.06	0.77	0.14	0.89	0.19	0.78
3	0.03	0.37	0.10	0.52	0.15	0.39
4	0.02	0.32	0.16	0.76	0.24	0.92
5	0.01	0.20	0.07	0.36	0.43	0.54
6	0.02	0.27	0.11	0.49	0.69	0.45
7	0.02	0.69	0.11	0.59	0.93	0.64
8	0.02	0.29	0.12	0.45	0.50	0.98

Table 3.7: SRF average error for 240 test inductors (in %)

	N=1	N=2	N=3	N=4	N=5	N=6	N=7	N=8
SRF	1.16	1.73	0.83	0.64	0.32	0.38	0.42	0.30

3.3. Integrated Inductor Synthesis Methodologies

In this section, several optimization algorithms are used in order to synthesize integrated inductors. The inductor optimization problem can be posed as a constrained optimization problem as described in Eq. (1.1). The synthesis of integrated inductors can be considered as a single-objective problem or

a multi-objective problem. In this Section, the Particle Swarm Optimization (PSO) algorithm [117] is used for single-objective optimization, and the Non-dominated Sorting Genetic Algorithm (NSGA-II) is used for multi-objective optimizations [118].

PSO is a single-objective population-based stochastic optimization technique, which was inspired is nature social behavior. The standard flowchart of PSO is shown in Fig. 3.12.

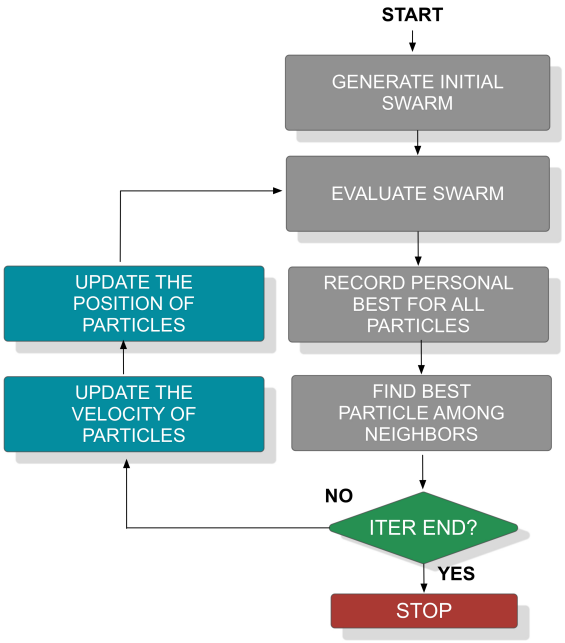


Figure 3.12: PSO flow chart.

The standard PSO algorithm is initialized with a population (called swarm) of candidate solutions (called particles). The particles that constitute a swarm, move around the search space, with a given $velocity$ (which is a parameter used to move from a position to another in the search space) looking for the best solution. Each particle has the ability of saving its current position, its historical best position, and the position of the neighboring particles [117]. During each iteration of the algorithm, the entire swarm is evaluated by an objective function (for inductors it could be the physical or surrogate model) to determine its *fitness* (the fitness is the value of the objective under optimization). Afterwards, the individual and global bests are updated. At this point, if the maximum number of iterations is achieved, the algorithm stops, if not, the velocity and position of each particle are updated. Each particle adjusts its traveling speed dynamically by taking into account its inertia, its historical best position and that of its best neighbor. These steps are repeated until some stopping condition is met (in this thesis the stopping condition is always the number of iterations imposed by the user).

The standard PSO algorithm was designed to only deal with unconstrained optimization problems. For inductor synthesis (or any circuit design problem) constraints are a must. Therefore, a tournament selection method [119] has been implemented in PSO to handle design constraints:

1. If two solutions do not comply with constraints, the one with the smallest constraint violation is

selected.

2. If one solution complies with constraints (denominated as a feasible point) and another does not (denominated as an infeasible point), the feasible point is selected.

3. If two feasible solutions are compared, the one with the best objective function value is selected.

For multi-objective optimizations, in this thesis, NSGA-II is adopted [118], whose flow is illustrated in Fig. 3.13.

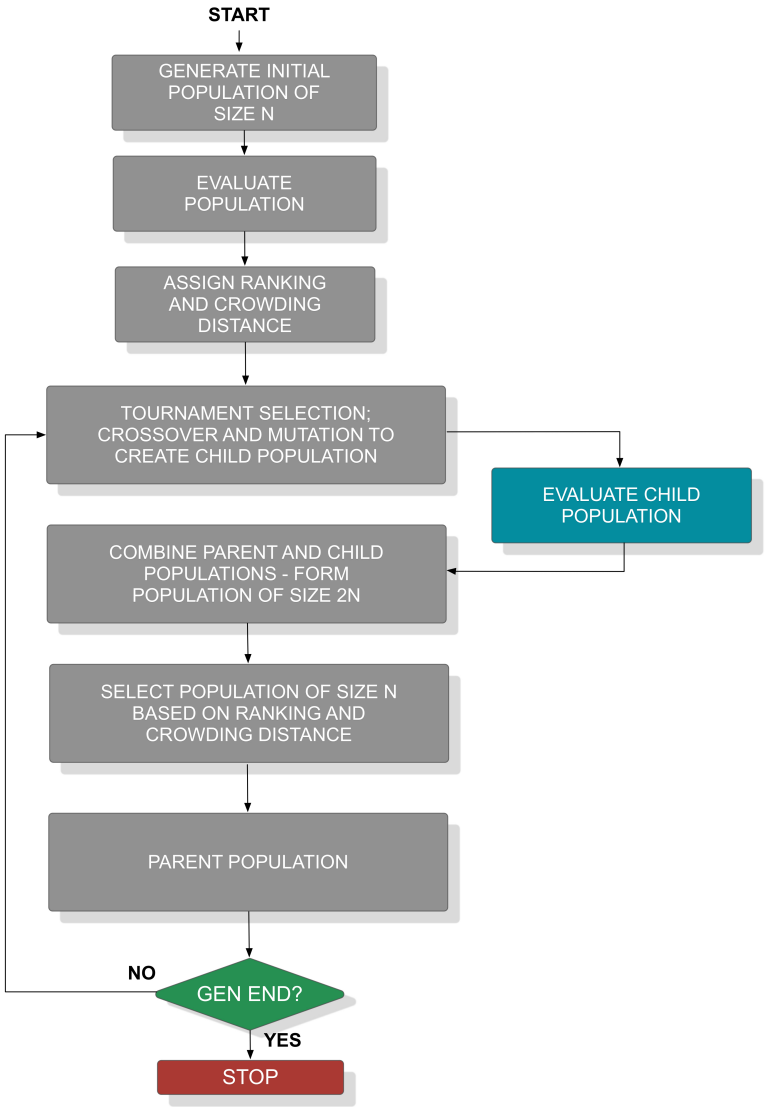


Figure 3.13: NSGA-II flow chart.

In the first step an initial population of N individuals is generated. Afterwards, these N individuals are evaluated in order to obtain the values of their objectives and constraints. In the next step (assign ranking and crowding distance, in Fig. 3.13), a classification process is performed in order to establish which are the most promising individuals. This process is denominated as $rank\ assignation$. In this process, all individuals are classified into fronts as follows: all non-dominated individuals are placed in

front 1 (F_1); individuals dominated by at least one individual of F_1, are placed in front 2 (F_2); individuals dominated by at least one individual of F_2, are placed in front 3 (F_3); and so on. While assigning the ranking, if any individual does not comply with constraints, the constraint violation in used to assign the rank. Afterwards, the crowding distance is also calculated. The crowding distance is a measure of how well distributed the solutions are in the performance space. This measure is especially interesting in multi-objective optimizations, because the user is usually looking to have a POF as wide and uniform as possible in order to cover all the performance space with different trade-offs.

After assigning ranks and calculating the crowding distance, all the individuals are taken four by four from the population (so-called parent population), and a tournament selection is performed. This tournament selection consists on a dominance check between pairs of individuals. If the individuals under comparison are both non-dominated, the one with larger crowding distance is selected. The selected individuals are then used to generate new individuals using the crossover operator.

Finally, the mutation operator performs random variations on the individuals. The population obtained after selection, crossover and mutation is denominated child population. This child population has to be evaluated in order to obtain its objectives and constraints, and, after that, it is combined with the previous parent population, in order to form a population with 2N individuals. After that, a survivor selection is performed by assigning the rank and calculating the crowding distance for the individuals, obtaining therefore, a new parent population. These steps are repeated until the number of generations imposed by the user is reached.

The synthesis of integrated inductors reported here, does not exploit any specific characteristics of PSO and NSGA-II, hence, they can be replaced by any other single-objective and multi-objective optimization algorithm, respectively. The basic optimization-based synthesis flow for integrated inductors is illustrated in Fig. 3.14. The synthesis strategies can be classified in four categories according to the kind of performance evaluator and how it interacts with the optimization technique. They will now be discussed in detail, highlighting their advantages and drawbacks.

1. EM simulation as a performance evaluator of an optimization technique (EMO):
   The EMO methods embed EM simulations to evaluate objectives and constraints within an optimization algorithm. Therefore, they provide the most accurate performance evaluation and, hence, the best solution quality of all methods. Their major drawback is the high computational cost of the EM simulations. This method constitutes an excellent comparison benchmark for other techniques.

2. Equivalent circuit model as a performance evaluator of an optimization technique (ECO):
   The ECO methods rely on a physical/analytical equivalent circuit model to obtain the performances of the passive component. Their main advantage is their high efficiency. However, it has been shown above that these models are usually not accurate enough for a passive component synthesis, showing errors typically much higher than 10%. Hence, when coupled with optimization algorithms, large deviations are observed on the synthesized passive

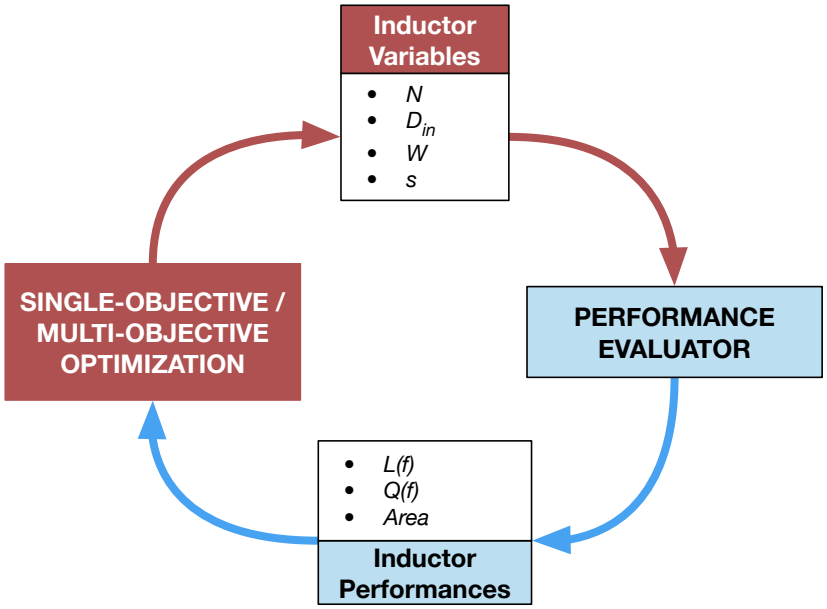


Figure 3.14: Optimization-based inductor synthesis loop

components when their performances are verified with EM simulation. Therefore, these models can only be used for a first order approximation and not for a full inductor synthesis.

3. Offline surrogate model as a performance evaluator of an optimization technique (OFFSO):
   With the OFFSO methodology, a global surrogate model is created before being used within an optimization algorithm [56]. The surrogate model is first built to be as accurate as possible. Then, the optimization algorithm uses this surrogate model as the performance evaluator to find the optimal solution. The surrogate model is called offline because training data can be generated by EM simulation and the model can be constructed before any optimization objectives and/or constraints are set. Normally, the data set used to build the surrogate model is generated covering the entire design space. When combined with an optimization algorithm, this method has the ability of searching through the entire design space in order to find a global optimum. The generation of the training data is computationally expensive. However, such training data is generated only once and is valid for any future optimization problem. Moreover, they can be generated offline, much before they are needed for the first inductor optimization problem. On the other hand, since the model can be evaluated very fast, the optimization process itself is highly efficient, usually in the range of few minutes.

4. Online surrogate model as a performance evaluator of an optimization technique (ONSO):
   Since global surrogate models may be locally inaccurate, ONSO methodologies, also known as surrogate-assisted evolutionary algorithms (SAEA), have received considerable attention, also in practical analog/RF circuit design problems [87]. In this methodology, a coarse surrogate model using a few training points is first constructed. Then, this coarse model is coupled with an

optimization algorithm and promising solutions (typically one) are electromagnetically simulated at each iteration of the optimization loop. The data from this EM simulation is used to update the surrogate model to make it more accurate in the region where new simulation points are added, while moving towards the presumed optimal inductor. However, the outputs of the ONSO methodology highly depend on the accuracy of the initial coarse model, which leads to two significant challenges for this methodology. First, the promising solutions found at the different iterations define the search space and the constructed surrogate model is only accurate in that space. Second, the success of ONSO comes from the basic assumption that the optimal point of the coarse and fine models are not far away in the design space. However, again, this assumption only holds when the coarse model is accurate enough. ONSO methods exhibit a delicate trade-off between efficiency and the probability of convergence to the global optimum. Better convergence can be achieved by either increasing the amount of training data of the coarse model, or emphasizing the exploration of potentially good regions of the design space during the optimization process, or a combination of both. In all cases, an increase in the number of EM simulations is implied, diluting in this way the efficiency advantage over EMO methods. A prescreening technique that can be used in ONSO methods in order to increase accuracy, consists in using the uncertainty measurement of the prediction, i.e., the mean square error (MSE), instead of just the predicted value to rank promising solutions. Such techniques include methods like lower confidence bound, probability of improvement or expected improvement (EI). The EI method, which is going to be used later in this Chapter, uses the MSE in order to evaluate areas of the design space that could be optimal considering the model error. Therefore, new promising solutions can be found by taking into account the MSE of the model.

Methods considering prescreening techniques have been widely applied for single-objective optimization [120, 121] and some more recent attempts have tried to extend these approaches to the multi-objective case [63, 122, 123]. Some of these approaches, especially the single-objective ones, have found their path to electronic circuit design application [87].

In the following sections, these approaches are examined and compared for the synthesis of integrated inductors.

3.3.1. Experimental Results: Single-Objective Optimizations

In this section, four different methodologies: EMO, OFFSO, ONSO and ONSO using expected improvement (for the sake of simplicity, further references to this method are denoted as ONSOEI) are applied to the synthesis of integrated inductors. The ECO methodology is not implemented since it was shown in Section 3.2.1 that physical models are not accurate at all, and, therefore, the optimization process yields suboptimal, and even invalid, inductors. The EMO method uses ADS *Momentum* as a performance evaluator and the OFFSO methodology uses the previously developed

surrogate model (using the independent N modeling and the SRF filtering strategy). The ONSO and ONSOEI methodologies have some differences when compared to the previous methods. The flow diagram of ONSO/ONSOEI is presented in Fig. 3.15.

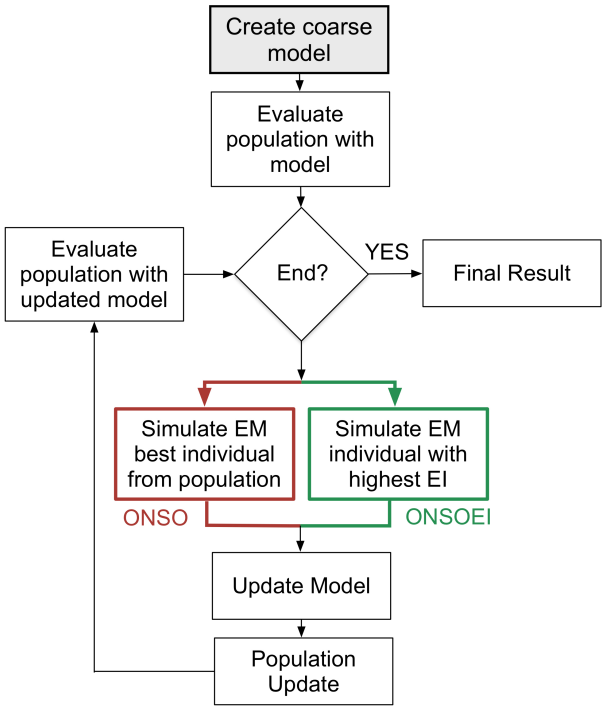


Figure 3.15: Flow Diagram of ONSO/ONSOEI

An initial surrogate coarse model is created using 40 (EM-simulated) training inductors. In this implementation of ONSO, the model is updated at each iteration with the EM simulation results of the best individual of the current population. In ONSOEI, the model is updated by simulating the inductor that presents the highest expected improvement from the current population. However, if any of these individuals (either the best one from the current population or that with the highest expected improvement) had already been simulated and used for the model construction in previous iterations, this individual is not EM-simulated and the model does not have to be updated in that iteration. The technology used for inductor synthesis was the same 0.35μm CMOS technology used for the model comparisons in Section 3.2. The bounds of the optimization search space are the same bounds of the samples used to create the surrogate models, and shown in Table 3.1.

The optimization constraints were defined to guarantee the ”good behavior” of the inductor at the frequencies of interest. The inductors have to be designed in such a way that they are in the so-called flat-bandwidth (BW) zone, as shown in Fig. 3.16 [55]. In order for the inductor to be in this zone, the inductance value must be sufficiently flat from DC (L_{DC}) to slightly above the operating frequency ($L_{eq}(f_o + \Delta f)$, where f_o is the operating frequency) and the self-resonance frequency must sufficiently above this frequency. Since in the EMO methodology it is extremely expensive to accurately calculate the SRF of the inductors, the latter constraint is approximated by imposing that the quality factor

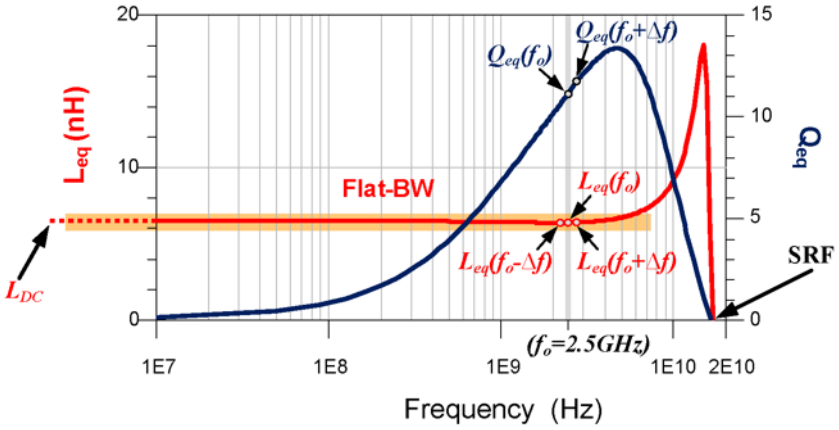


Figure 3.16: Flat bandwidth zone.

at the operating frequency ($Q_{eq}(f_o)$) is near its maximum and always with a positive slope around it (($Q_{eq}(f_o+\Delta f)$-$Q_{eq}(f_o)$>0) [55]. In order to constrict the area, a constraint is added so that the inductor fits within a 400μmx400μm square. Therefore, the optimization constraints are formulated as:

$$area < 400\mu m \times 400\mu m \tag{3.43}$$

$$\left|\frac{L_{at2.5GHz} - L_{at2.55GHz}}{L_{at2.5GHz}}\right| < 0.01 \tag{3.44}$$

$$\left|\frac{L_{at2.5GHz} - L_{at2.45GHz}}{L_{at2.5GHz}}\right| < 0.01 \tag{3.45}$$

$$\left|\frac{L_{at2.5GHz} - L_{at0.1GHz}}{L_{at2.5GHz}}\right| < 0.05 \tag{3.46}$$

$$Q_{at2.55GHz} - Q_{2.5GHz} > 0 \tag{3.47}$$

Eq. (3.46) is used in order to guarantee that the inductor is in the flat-BW zone, by ensuring less than 5% deviation between 0.1GHz and f_o (in this example set at 2.5GHz). Eqs. (3.44) and (3.45) guarantee that the inductance is very flat around f_o.

Furthermore, Eq. (3.47) is used in order to guarantee a positive slope in the quality factor around f_o, which is used to ensure that the SRF is still far away. To have a fair comparison with the other methods, and although it was not strictly necessary (because an SRF model was developed with the surrogate), the constraint related to the SRF location was imposed identically in all methods. The objective of the first test is to find an octagonal inductor with $L_{spec} = 2nH$ at 2.5GHz while maximizing the quality factor. Since PSO is a single-objective algorithm, a weighted objective function was built so that the quality factor was maximized and the difference between the desired inductance and the one obtained by the algorithm was minimized:

$$f(x) = -Q(x) + \lambda|L(x) - L_{spec}| \tag{3.48}$$

where λ is set to 5. Results for the best inductor obtained by a single execution of each methodology are shown in Table 3.8. The performances of such optimal inductors have been electromagnetically simulated a posteriori, so that the L and Q values shown at the table can be fairly compared.

Table 3.8: Results of one execution with all methods targeted at $L = 2nH$ and maximizing Q. Area< 400μmx400μm

Method	N	D_{in} (μm)	w (μm)	Performances L (nH)	Q	EM sims.	CPU time
EMO	2	225	14.15	1.999	11.086	8000	106.5 h.
ONSO	2	225	14.10	1.999	11.073	45	32 min.
ONSOEI	2	225	14.10	1.999	11.073	55	56 min.
OFFSO	2	225	14.10	1.999	11.073	0	2 min.

It must also be considered that the time data in Table 3.8 correspond to CPU time. The computer used for all simulations had two 6-core Intel® Xeon® E5-2630 v2 processors at 2.60GHz, enabling parallelization of the evaluation of different solutions. Such parallelization is very effective for the EMO approach, achieving a reduction of elapsed time by about a 10x factor with respect to the CPU time. A priori, parallelization of the OFFSO approach is not worth given the total CPU times involved. Model updating in ONSO and ONSOEI is performed with at most one inductor at each iteration, and, therefore such parallelization is not directly possible.

Notice that the number of EM simulations, and, therefore, the computation times for the OFFSO, ONSO and ONSOEI methods only include the simulations performed during the execution of the PSO algorithm. Construction of the initial coarse model in ONSO and ONSOEI requires another 40 simulations (5 for each number of turns). This takes another 23.11 hours of CPU time. The CPU time required to simulate the 800 training samples in OFFSO amounts to 462.30 hours (around 19 days). Indeed, as stated above, parallelization of these evaluations in the machine with two 6-core processors reduces the elapsed time by approximately a factor 10x with respect to the CPU time. Since the initial 40 EM simulations for the coarse model in ONSO and ONSOEI and the 800 samples for the OFFSO method can be run a priori and it is a one-time investment (they are independent of the required optimization objectives), they have not been included in the CPU time calculation of the optimization process shown in the table. The table only reflects the CPU time required to get the optimization results once the optimization goals are known. This means that the initial accurate simulations should not be accounted as time to build a given model as they are only performed once and can be used to build several different models using different techniques. To understand the lack of proportionality between the CPU times above and those in the table, two considerations must be made:

1. Some simulations for the initial sampling take longer, since simulations of inductors with 8 turns require much more time than e.g. 3 turns, whereas convergence of the different methods in this example implies that most additional EM simulations correspond to inductors with less than 4 turns

2. The EM simulations of the 40 samples of the coarse model in ONSO and ONSOEI and the 800 samples in OFFSO were performed for several hundreds of frequency points so that the results can be used for any synthesis problem independently of the frequencies of interest. If only the few frequency points necessary for this experiment were used, the CPU time is reduced from 23.11 hours to 1.22 hours, and from 462.30 hours to 24.36 hours respectively. However, in that case, new samples and their corresponding EM simulation are needed whenever a new frequency of operation is desired.

As an illustration example, the performances of the inductor obtained with the OFFSO methodology in the first test example (Table 3.8) are presented in Fig. 3.17 and they are compared against the EM simulation of the same inductor. It is possible to observe that the accuracy of the model is remarkably good along all the frequency range. After the optimization process (which takes 2 minutes) the inductor synthesis is complete and the layout of this inductor is presented in Fig. 3.18.

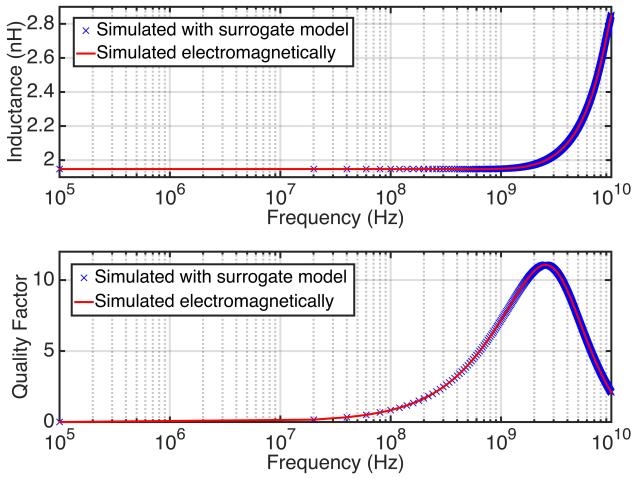


Figure 3.17: Performance parameters of the 2nH inductor obtained in the first test example: inductance and quality factor vs frequency curves

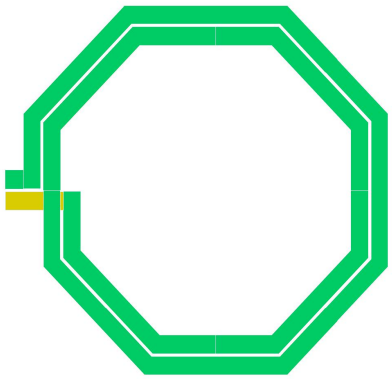


Figure 3.18: Layout of the 2nH inductor obtained in the first test example

The results for another experiment, this time addressing an inductor with 2.5nH and maximum quality factor at 2.5GHz, are shown in Table 3.9.

Table 3.9: Results of one execution with all methods targeted at $L = 2.5nH$ and maximizing Q. Area< 400μmx400μm

Method	N	D_{in} (μm)	w (μm)	Performances L (nH)	Q	EM sims.	CPU time
EMO	2	260	10.60	2.504	10.704	8000	111.2 h.
ONSO	3	136	9.50	2.500	10.390	36	34.3 min.
ONSOEI	2	259	10.35	2.499	10.713	59	67.6 min.
OFFSO	2	260	10.80	2.498	10.742	0	2 min.

As in any other computational intelligence algorithm, PSO also implies the introduction of randomness, and, hence, different runs may provide different results. Therefore, 20 independent runs were performed for each experiment. The mean values and standard deviations obtained with the different techniques are shown in Table 3.10 and Table 3.11.

Table 3.10: Mean values and standard deviations (between brackets) with all methods targeted at $L = 2nH$ and maximizing Q. Area< 400μmx400μm

Method	Performances L (nH)	Q	EM sims.	CPU time
EMO	1.999 (0.000)	11.08 (0.000)	8000 (0.0)	106.5 (0.0) h.
ONSO	1.999 (0.000)	11.073 (0.000)	45 (0.0)	32 (0.0) min.
ONSOEI	1.999 (0.000)	11.073 (0.000)	55 (0.0)	56 (0.0) min.
OFFSO	1.999 (0.000)	11.073 (0.000)	0	2 (0.0) min.

Table 3.11: Mean values and standard deviations (between brackets) with all methods targeted at $L = 2.5nH$ and maximizing Q. Area< 400μmx400μm

Method	Performances L (nH)	Q	EM sims.	CPU time
EMO	2.502 (0.001)	10.650 (0.102)	8000 (0.0)	111.2 (0.0) h.
ONSO	2.500 (0.001)	10.390 (0.335)	35.9 (8.0)	34.3 (8.3) min.
ONSOEI	2.499 (0.008)	10.713 (0.265)	62.2 (33.1)	67.6 (36.0) min.
OFFSO	2.498 (0.010)	10.742 (0.144)	0	2 (0.0) min.

From the comparison of these results of the different techniques for single-objective optimization, several conclusions can be drawn:

1. OFFSO converges to approximately the same solutions than the reference method EMO in all cases. However, the efficiency is drastically increased, since the CPU time decreases from more than 100 hours to roughly 2 minutes. These test examples demonstrate that the accuracy of the surrogate model used in the OFFSO methodology leads to the same design space areas with much higher efficiency.

2. All methods practically converge to the same solutions in the 2nH example but a larger variability between different executions appears for the 2.5nH example in ONSOEI and especially ONSO, yielding a slightly lower quality factor. This seems to indicate that despite the EM simulations used in order to iteratively increase the accuracy of ONSO, the accuracy of the initial coarse model is crucial for an optimal inductor synthesis, i.e. if during the first iterations, where the model is still quite inaccurate, the optimization algorithm leads to design space areas away from the optimal point, it is less likely that the optimization algorithm will converge to the global optimum. Moreover, the computation time rises to tens of minutes due to the additional EM simulations. The use of the expected improvement in ONSOEI improves, in most cases, the ONSO ability to locate the optimal regions of the search space and, therefore, the accuracy of the method is quite good. However, the use of this prescreening method brings a penalty in the form of additional EM simulations that typically rises the optimization time to about one hour.

In the examples shown above, the OFFSO, ONSO and ONSOEI methodologies converge to the same solutions either if the training inductors with SRF close or below the frequency of operation are filtered out according to the two-step modeling method described above or not. Inductors with a number of turns $N \leq 3$ are obtained. All training inductors with these numbers of turns have a SRF sufficiently above 2.5GHz. Therefore, it becomes natural that the effect of the SRF filtering methodology previously proposed is negligible. However, when the specs are such that they are met with inductors with a larger number of turns, they tend to have smaller SRF and the effect of the proposed modeling approach becomes more noticeable. To show this, we will consider the comparison to methods similar to OFFSO, ONSO and ONSOEI, but in which all inductors are used in the training phase of the L/Q model, i.e, no inductor is filtered out if its SRF is close or below 2.5GHz. Correspondingly, we will denote these methods as OFFSO$_{NF}$, ONSO$_{NF}$ and ONSOEI$_{NF}$.

In a first example, an inductor of 2.9nH with maximum quality factor that fits into a 125μmx125μm square is requested. Identical performance constraints to the previous examples are imposed. The results for one execution are shown in Table 3.12. In this case, OFFSO and OFFSO$_{NF}$ arrive at different results. Moreover, when the resulting inductors are EM-simulated, the performance constraints in OFFSO$_{NF}$ are not met any more. ONSO, ONSOEI and ONSOEI$_{NF}$ arrive at results similar to OFFSO, but ONSO$_{NF}$ is unable to converge to a feasible solution (as indicated in the fifth column in Table 3.12). A second example is shown in Table 3.13. In this case an inductance of 4.6nH with maximum quality factor within a 140μmx140μm square is specified. In this case, all methods but EMO and OFFSO are unable to converge to a solution due to the larger errors of the surrogate models of inductance and quality factor.

As in the previous experiments, 20 executions of each algorithm were performed for both cases. The statistical analysis of the results is shown in Table 3.14 and Table 3.15. The second column in these tables shows how many of the 20 executions the optimization algorithm found a feasible solution. The statistical analysis of L and Q has been performed only for the feasible solutions found. It can be

Table 3.12: Results of one execution with all methods targeted at $L = 2.9nH$ and maximizing Q. Area< 125μmx125μm

Method	N	Din (μm)	w (μm)	Feasible solutions found?	Performances		EM sims.	Constraints met after EM sim?	CPU time
					L (nH)	Q			
EMO[a]	6	36	5.15	yes	2.90	8.45	8000	yes	418.5 h.
ONSO	6	35	5.45	yes	2.89	8.49	9	yes	32.2 min.
ONSO$_{NF}$	4	70	5	no	-	-	2	-	4.2 min.
ONSOEI	6	35	5.45	yes	2.89	8.49	45	yes	111.2 min.
ONSOEI$_{NF}$	6	35	5.45	yes	2.89	8.49	45	yes	111.2 min.
OFFSO	6	37	5.3	yes	2.98	8.55	0	yes	2 min.
OFFSO$_{NF}$	6	40	5	yes	3.11	8.59	0	no	2 min.

[a]The elapsed time in EMO reduces by a factor 10 with respect to the CPU time when all cores of the twin 6-core processor are used.

Table 3.13: Results of one execution with all methods targeted at $L = 4.6nH$ and maximizing Q. Area< 140μmx140μm

Method	N	Din (μm)	w (μm)	Feasible solutions found?	Performances		EM sims.	Constraints met after EM sim?	CPU time
					L (nH)	Q			
EMO[a]	7	40	5.05	yes	4.56	8.616	8000	yes	590.5 h.
ONSO	5	70	5	no	-	-	3	-	6.8 min.
ONSO$_{NF}$	5	70	5	no	-	-	3	-	7.5 min.
ONSOEI	6	55	5	no	-	-	5	-	12.4 min.
ONSOEI$_{NF}$	5	70	5	no	-	-	9	-	11.4 min.
OFFSO	7	40	5	yes	4.54	8.520	0	yes	2 min.
OFFSO$_{NF}$	6	55	5.05	no	-	-	0	-	1.5 min.

[a]The elapsed time in EMO reduces by a factor 10 with respect to the CPU time when all cores of the twin 6-core processor are used.

checked in Table 3.14 that ONSOEI arrives to similar solutions than OFFSO, although with a penalty in the computation time. ONSO$_{NF}$ never arrives at a feasible solution, like in the single execution shown in Table 3.12. It is also found that ONSO and ONSOEI$_{NF}$ only converge to a solution about half of the executions. Table 3.15 shows that only EMO and the proposed OFFSO approach always converge to a solution and they are quite similar, but with orders of magnitude less computational effort in the OFFSO case.

Table 3.14: Mean vaues and standard deviations (between brackets) with all methods targeted at $L = 2.9nH$ and maximizing Q. Area<125μmx125μm

Method	Feasible solutions found?	Performances		EM sims.	Constraints met after EM sim?	CPU time
		L (nH)	Q			
EMO[a]	20/20	2.904 (0.000)	8.421 (0.000)	8000 (0.0)	20/20	418.5 (0.0) h.
ONSO	11/20	2.891 (0.000)	8.488 (0.000)	9.33 (6.02)	11/20	32.2 (0.0) min.
ONSO$_{NF}$	0/20	-	-	2 (0.0)	0/20	4.2 (0.0) min.
ONSOEI	20/20	2.890 (0.002)	8.483 (0.022)	45 (0.0)	20/20	111.2 (0.0) min.
ONSOEI$_{NF}$	13/20	2.889 (0.004)	8.422 (0.182)	37.1 (15.1)	13/20	95.2 (37.5) min.
OFFSO	20/20	2.986 (0.004)	8.545 (0.018)	0	20/20	2 (0.0) min.
OFFSO$_{NF}$	20/20	3.110 (0.000)	8.590 (0.000)	0	0/20	1.5 (0.0) min.

[a]The elapsed time in EMO reduces by a factor 10 with respect to the CPU time when all cores of the twin 6-core processor are used.

Table 3.15: Mean values and standard deviations (between brackets) with all methods targeted at $L = 4.6nH$ and maximizing Q. Area<140μmx140μm

Method	Feasible solutions found?	Performances		EM sims.	Constraints met after EM sim?	CPU time
		L (nH)	Q			
EMO[a]	20/20	4.562 (0.017)	8.564 (0.131)	8000 (0.0)	20/20	590.5 (0.0) h.
ONSO	0/20	-	-	4.15 (2.5)	0/20	9.4 (4.4) min.
ONSO$_{NF}$	0/20	-	-	3 (0.0)	0/20	7.1 (0.4) min.
ONSOEI	0/20	-	-	5 (0.0)	0/20	12.4 (0.0) min.
ONSOEI$_{NF}$	0/20	-	-	6.8 (2.0)	0/20	12.0 (0.5) min.
OFFSO	20/20	4.540 (0.007)	8.530 (0.029)	0	20/20	2 (0.0) min.
OFFSO$_{NF}$	0/20	-	-	0	0/20	1.5 (0.0) min.

[a]The elapsed time in EMO reduces by a factor 10 with respect to the CPU time when all cores of the twin 6-core processor are used.

From the latter experiments, it can be concluded that in many cases the proposed two-step surrogate modeling strategy plays a key role in the proper convergence and accuracy of the surrogate-based optimization techniques for inductor synthesis.

3.3.2. Experimental Results: Multi-Objective Optimizations

One of the advantages of having a fast and accurate surrogate model that needs no EM simulations during the optimization process is the ability of using this model within a multi-objective optimization algorithm. Given the lower maturity of ONSO-like multi-objective optimization techniques and the fact that already for single-objective optimization of inductors, the ONSO and ONSOEI methodologies have not provided better solutions than the OFFSO approach and always with a higher computation time, this section will compare the OFFSO and EMO methodologies with multi-objective optimization algorithms. The effect of the two-step modeling approach will be also studied. The search space is the same used in the previous optimizations and shown in Table 3.1. As a first test example, an optimization with two objectives was performed. The optimization problem had two objectives: inductance and quality factor maximization. Furthermore, the inductors should comply with the constraints described in Eq. (3.43)-(3.47).

This optimization was performed with 300 individuals and 100 generations. The results are presented in Fig. 3.19, where the results of the optimization using the surrogate model have been electromagnetically simulated so that the accuracy can be fairly compared. It is possible to observe that the Pareto fronts obtained by both methods are very similar. The advantage of using OFFSO is the efficiency. While with EMO the optimization lasted 355.55 hours (around 15 days CPU time)[1], the OFFSO method lasted 4 minutes, which is an increase in efficiency of about three orders of magnitude.

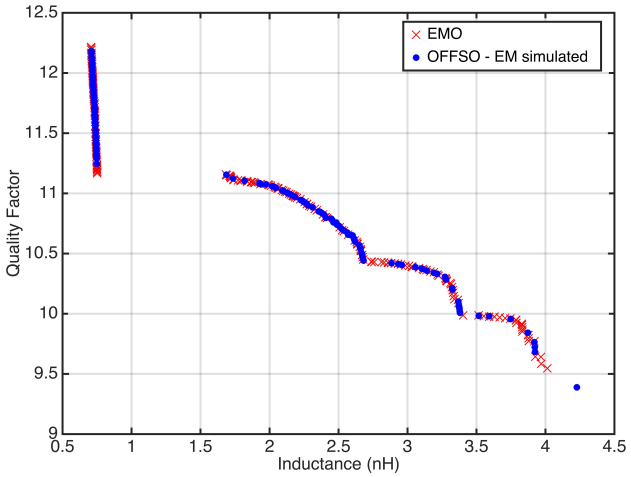


Figure 3.19: Pareto-optimal front for a two objective optimization, maximizing quality factor and inductance.

A second test example was an optimization with 3 objectives, this time with 1000 individuals and 80 generations. Since area is of great importance especially in IC technologies, area minimization was added as a third objective in the optimization. A major motivation for selecting a large population size is that the application of inductor fronts to RF circuit design benefit from denser Pareto fronts [35].

[1]The elapsed time reduces to 29 hours with respect to the CPU time when all cores of the twin 6-core processor are used.

The results are shown in Fig. 3.20. The results of the surrogate model that are shown in Fig. 3.20 have been electromagnetically simulated a posteriori so that both fronts can be fairly compared.

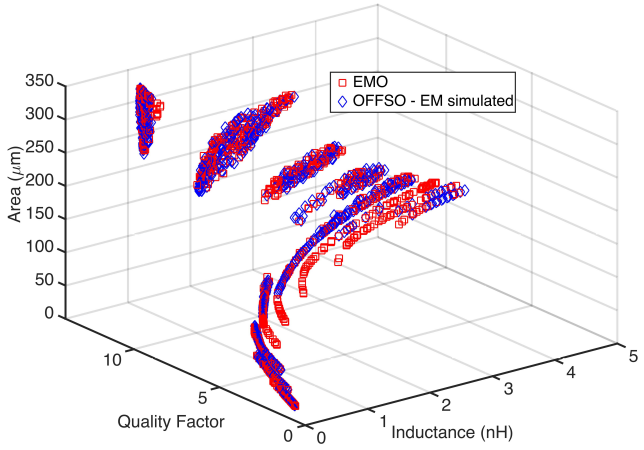


Figure 3.20: EM simulation of Pareto-optimal fronts for a 3 objective optimization, maximization of quality factor and inductance and minimization of area using EMO and OFFSO methods.

Again, the Pareto fronts achieved by both methods are very similar, and its comparison is very difficult. For single-objective optimization algorithms, comparing two solutions given by two different optimization processes is simple because one just has to compare the fitness function (the objective value). For 2D problems, by drawing two given POFs and inspecting them (e.g., Fig. 3.19) it is still relatively easy to see which POF dominates the other. However, this is not the case for 3D multi-objective algorithms, where hundreds of solutions are given as a POF in a 3D space. Therefore, in order to perform a comparison between POFs, a more accurate comparison should be performed by using performance metrics, specifically developed for this purpose. In this thesis, two different metrics will be used: hypervolume and coverage set. The hypervolume metric given an insight on diversity and convergence the POF is, while the coverage set allows performing binary comparisons between two fronts, as it gives the percentage of points of each front dominated by the other one [124].

The hypervolume is basically a calculation of the union of the hypercubes determined by each solution in the objective space and a reference point (see Fig. 3.21). A feature of the hypervolume metric is that it does not require any knowledge of the true Pareto front, which especially convenient in our engineering problem in which the true Pareto front is not known. The hypervolume metric depends on the selected reference point, hence, the same reference point must be used in both cases, in order to fairly compare the Pareto fronts generated with the two different techniques.

Furthermore, given two solution sets, P_1 and P_2, the set coverage is defined as:

$$C(P_1, P_2) = \frac{|\{b \in P_2 | \exists a \in P_1, a \prec b\}|}{|P_2|} \tag{3.49}$$

where $a \prec b$ means that a dominates b. A similar value of $C(P_1, P_2)$ and $C(P_2, P_1)$ implies that no front is better than the other. In practice, given two solution sets, P_1 and P_2, the set coverage is defined as

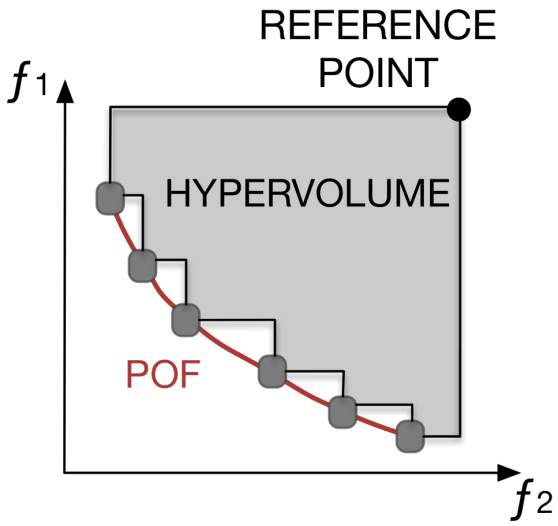


Figure 3.21: Illustrating the hypervolume calculation.

$C(P_1, P_2)$, which is the ratio of solutions in P_2 that are dominated by at least one solution in P_1, e.g., if $C(P_1, P_2)$=1, it means that all solutions in P_2 are dominated by P_1.

The hypervolume of the Pareto front obtained with the EMO approach was HV_{EMO}=10674 and that with the OFFSO approach (after electromagnetically simulating the final results) was HV_{OFFSO}=10604, which is very similar. Regarding the set coverage, the calculated figures were:

$C(PF_{EM}, PF_{OFFSO}) = 0.16$

$C(PF_{OFFSO}, PF_{EM}) = 0.14$

that indicates that practically the same percentage of points are dominated by the other front.

The EMO optimization took 1926.39 hours (roughly 80 days CPU time)[2] while the OFFSO lasted 7 minutes, which is an incredible increase in efficiency while obtaining very similar Pareto fronts due to the accuracy of the surrogate model. It is also interesting to compare the results with those of the optimization using the surrogate model without the first filtering stage, i.e., the $OFFSO_{NF}$ methods. Fig. 3.22 compares the results of the EMO approach and the $OFFSO_{NF}$ approach (after electromagnetically simulating the final results). There are areas of the Pareto front that are not found with the surrogate-based optimization (infeasible points are not plotted). These areas mostly correspond to inductors with larger number of turns, where the SRF is considerably lower and the SRF filtering approach becomes more noticeably for the 2.5GHz operating frequency.

The hypervolume of the Pareto front obtained now with the $OFFSO_{NF}$ approach (after electromagnetically simulating the final results) was $HV_{OFFSO_{NF}}$=9626, which is clearly inferior to the EMO and OFFSO approaches. Regarding the set coverage, the calculated figures were:

$C(PF_{EM}, PF_{OFFSO_{NF}}) = 0.22$

$C(PF_{OFFSO_{NF}}, PF_{EM}) = 0.13$

that indicates that the quality of the surrogate model has clearly decreased. It is possible to conclude

[2]The elapsed time reduces to 144 hours when all cores of the twin 6-core processor are used.

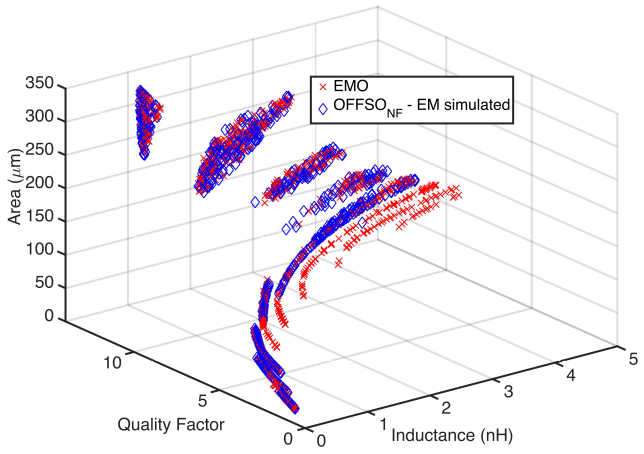


Figure 3.22: EM simulation of Pareto-optimal front for a 3 objective optimization, maximization of quality factor and inductance and minimization of area using EMO and OFFSO$_{NF}$ methods.

that the application of surrogate modeling strategies can enhance the efficiency-accuracy trade-off of conventional analytical or EM-based inductor optimization techniques for RF integrated circuits. The new two-step surrogate modeling strategy dramatically improves the modeling accuracy of integrated inductors.

It can be concluded, that prescreening techniques can be used in surrogate-assisted optimization techniques in order to achieve similar results to EM-based approaches with a significantly lower computation time. However, it is also found that similar or better results are obtained if offline surrogate models with a sufficient number of inductor samples are created following the proposed modeling strategy. Much lower CPU times must be invested during the optimization process since expensive EM simulations are not performed during the optimization stage. The quality of the results of the proposed strategy is also competitive in multi-objective optimization problems, whereas orders of magnitude computation time is saved.

3.4. SIDe-O: A Tool for Modeling and Optimization of Integrated Inductors

During the past few years, an immense effort has been made by the research community for the development of CAD tools for RF circuit design [125]. CAD tools for the design of integrated inductors have been reported in literature, such as ASITIC [126] or SISP [101]. However, these tools are based on physical/analytical models, which typically present accuracy issues in some design space areas and at higher frequencies, as was shown in the previous Section. Currently, foundries and EDA companies provide tools for inductor design and optimization, but with some drawbacks: either analytical models are used to model inductors, presenting accuracy issues, or limited optimization options are provided

to the user. More commercial tools such as Helics' VeloceRF are also available on the market. This tool provides accurate models based on an electromagnetic engine (more expensive simulations) and the tool allows inductor optimization, but also with limited options (only maximization of the quality factor). Furthermore, no available tool allows multi-objective optimizations, which may be very useful nowadays for obtaining design trade-offs for a given technology and performing design space exploration.

In this section a new MATLAB toolbox, called SIDe-O, is presented [127]. This toolbox provides accurate inductor models (based on the surrogate modeling techniques previously presented), diverse and complex optimization options and is, to the best of the author's knowledge, the first tool to ever allow multi-objective optimization of integrated inductors. The toolbox presented in this Section won the SMACD 2016 electronic design automation competition.

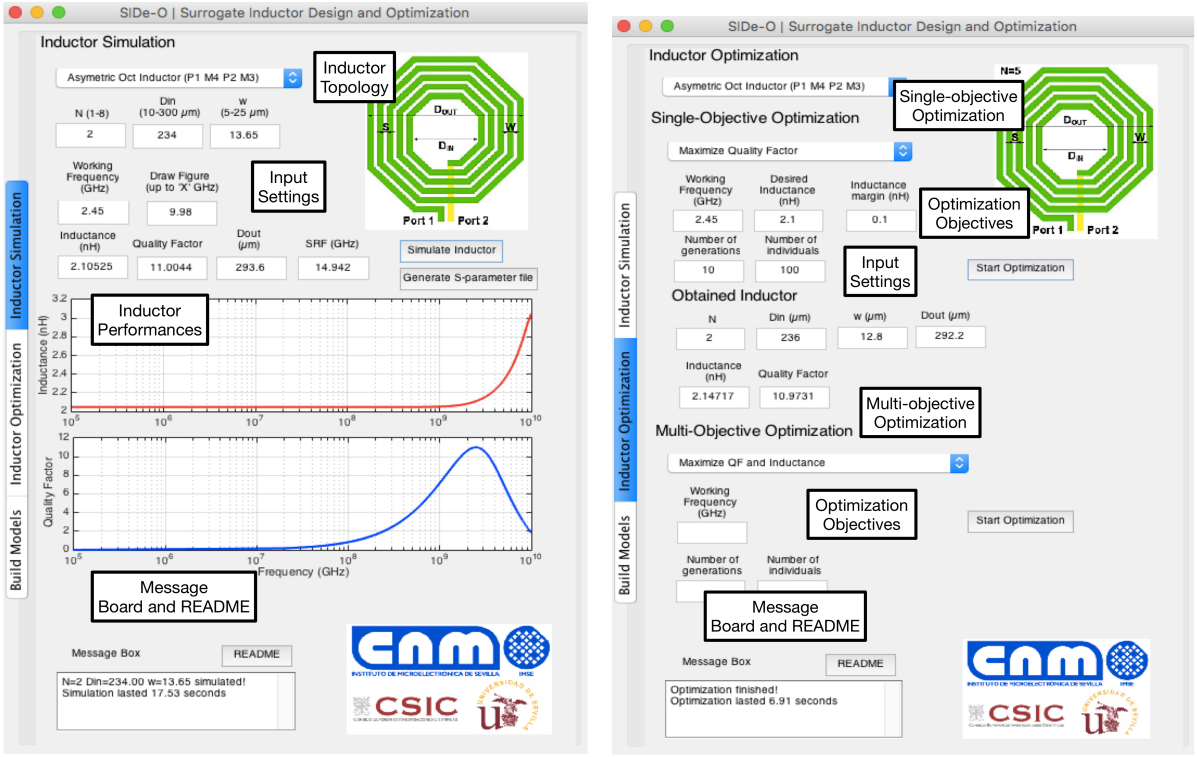
3.4.1. Designer Interface

In this section, only an introduction to the designer interface of the toolbox is given, as the fundamental techniques have been described in previous Sections. The complete designer interface can be observed in Fig. 3.23. The surrogate models used in the toolbox were developed in MATLAB, therefore, for a straightforward integration, the graphical user interface (GUI) was also developed in MATLAB. The GUI is multi-tabbed, with each tab suited for a different operation.

The first tab in Fig. 3.23a, $Inductor\ Simulation$, allows the user to simulate different inductor topologies, for a given working frequency and also to draw the inductance and quality factor curve along the entire frequency range for which the models are built.

The second tab in Fig. 3.23b, $Inductor\ Optimization$, allows the user to perform single- and multi-objective optimization of inductors. In single-objective optimization, the objectives of the optimization can be changed. The tool allows the user to maximize the quality factor, minimize the area, or both (by means of a weighted function where the weights of the function can be selected by the user) while achieving a given inductance. The multi-objective optimization can be performed either with two different sets of objectives: a two-objective optimization, maximizing quality factor and inductance, or a three-objective optimization, where quality factor and inductance are maximized and area is minimized. In both optimization algorithms, constraints are applied in order to guarantee that the selected inductors can operate at the chosen working frequency (WF). These constraints are specified in Eqs. (3.43)-(3.47).

The third tab in Fig. 3.23c, $Build\ Model$, allows the user to build his/her own models for other technology processes or inductor topologies, by providing a training set for the surrogate modeling. By providing a test set it is also possible to validate the model automatically with the tool. Afterwards, the mean relative errors of the model are shown in a table for immediate model validation. Moreover, once the new model is built, it is automatically included as an option in the topologies popup menu of the other tabs and suitable for immediate simulation and optimization. All tabs have a message board and a README file, which are appropriate for an easy tool usage. The tool allows the user to



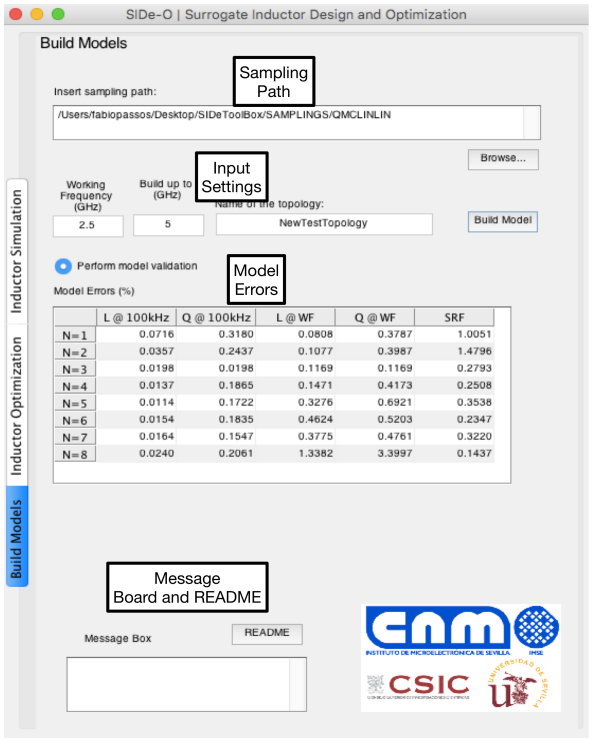


Figure 3.23: SIDe-O graphical user interface (GUI) shown in separate tabs. (a) Tab for inductor simulation. (b) Tab for inductor optimization. (c) Tab to build new inductor models.

generate an S-Parameter file for any given inductor. This S-Parameter file can afterwards be used in a modern simulator, such as HspiceRF or SpectreRF for an accurate description of the inductor behavior. For example, the AnalogLib library of Cadence has a device particularly for this purpose, the $nport$.

The SIDe-O tool, presented is this Section, will be further used in this thesis in order to model inductors in several optimization-based circuit design methodologies.

7

Conclusions

The design of RF circuits is highly complex, with difficult to manage and convoluted trade-offs. The usage of systematic design methodologies can help to design these RF circuits more efficiently, hence reducing the time-to-market. This was the main topic of this dissertation: to focus on the development of new systematic design methodologies capable of improving the state-of-the-art, cut short the distance between the RF and digital automatic design tools and reducing the time-to-market, therefore, shortening the existing productivity design gap in RF circuit design. In order to establish a methodology which is able to accurately design RF circuits, several bottlenecks of the RF design were tackled in this thesis. One of the most well-known bottlenecks in RF design, is the accurate, and efficient, modeling of integrated inductors.

In this thesis, a state-of-the-art surrogate modeling strategy for integrated inductors was developed. The presented model has less than 1% error when compared to EM simulations, while reducing the simulation time by three orders of magnitude. Several different models were created for different inductor topologies, all of them achieving negligible errors when compared to EM simulations. Due to the accurate and efficient surrogate model developed, its usage in optimization methodologies is encouraged. In this thesis, several different inductor synthesis strategies were compared. From this comparison it was possible to conclude that building an accurate global surrogate model shows very significant advantages when compared to state-of-the-art surrogate-assisted optimization strategies (ONSO and ONSOEI). Furthermore, a tool for the design and optimization of integrated inductors, SIDe-O, was developed. SIDe-O also allows the creation of S-parameter files that accurately describe the behavior of inductors for a given range of frequencies, which can later be used in electrical simulations for circuit design in commercial environments. The surrogate models developed, and integrated in the tool, provide a solution to the problem of accurately and efficiently modeling and optimizing inductors,

which alleviates the bottleneck that these devices represent in the RF circuit design process.

In this thesis, bottom-up design methodologies were applied to the design of RF circuits, starting from the lowest possible level: device level. The methodology uses the developed SIDe-O tool in order to generate Pareto fronts of inductors, which can later be used in circuit simulations. Furthermore, several different simulation strategies are used in order to reduce the circuit simulation time. By using such strategies some of the most expensive RF performances (e.g., third-order intercept point) can be efficiently calculated and considered during the automated design of RF circuits. Furthermore, since in RF the layout parasitics are so destructive, a layout-aware methodology was developed specifically for the design of RF circuits. The methodology uses multi-objective optimization algorithms and a bottom-up design methodology. An automatic layout generation is performed during the optimization for each sizing solution using a state-of-the-art module generator, template-based placer and router, which were specifically developed for RF circuits. The proposed approach exploits the full capabilities of most established computer-aided design tools for RF design available nowadays, such as the RF circuit simulator as performance evaluator and commercial layout parasitic extractor to determine the complete circuit layout parasitics. Furthermore, the inductor parasitics are considered using the previously developed surrogate model. The methodology developed also allows the user to consider the corner performances during not only the sizing optimization, but also during the layout-aware optimization, increasing therefore the design robustness. Finally a multilevel bottom-up strategy was illustrated and applied to RF circuits for the first time. By using such multilevel bottom-up strategy, different circuits can be connected in order to build an RF system. Furthermore, each level of the hierarchy is simulated with the upmost accuracy possible: EM accuracy at device level and transistor-level simulations at circuit/system level. Moreover, the methodology encourages the hierarchical low-level POF reuse, which is typical in bottom-up methodologies.

In summary, this thesis presented a new multilevel approach to design RF systems, where the system is designed in a bottom-up fashion, starting from the device level stage. Furthermore, at each stage of the design hierarchy, several aspects are taken into account in order to increase the design robustness, such as: inductor accurate characterization, layout parasitics and process variability.

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